

Measurements of Analog to Digital Converter Differential Non-Linearity

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Summary:

This paper documents Differential Non-Linearity (DNL) measurements of prospective Analog to Digital Converters (ADCs) for the GLAST calorimeter. Prospective ADCs are those that have 12 bits or greater resolution and are low-power switched-capacitor ADCs with serial data outputs. From the measurements that we made, the MAX189 12 bit ADC has the best 12-bit resolution.

Introduction:

With the availability of low-power switched-capacitor ADCs, the GLAST calorimeter is designed to have one ADC per log end. Selection of the particular ADC to be used will partially be determined by the DNL of the device. Seven devices are tested:

<u>Manufacturer</u>	<u>Part Number</u>	<u>Resolution</u>
Maxim	MAX189	12 bit ADC
Maxim	MAX1241	12 bit ADC
Maxim	MAX145	12 bit ADC
Burr-Brown	ADS7816	12 bit ADC
Analog Devices	AD7475	12 bit ADC
Burr-Brown	ADS8320	16 bit ADC
Maxim	MAX194	14 bit ADC

For comparison, DNL plots are shown with reduced resolution down to 11 bits.

Setup:

A circuit board previously designed to test prototype analog ASIC chips with various ADCs was used for the testing. A Xilinx FPGA residing on the circuit board controlled the selected ADC and transferred the data to a PC computer. A slow ramp triangle wave was applied to the input of the ADC while a faster periodic signal created triggers for the sampling and conversion. Each ADC was separately run long enough to gather sufficient statistics. When running, the ADC is in low power sleep mode prior to trigger, and given enough time to ‘wake up’ (few microseconds) prior to conversion. An IDL program was used to plot the results.

DNL Measurements:

12 BIT ADCs.

Figure 1 Maxim MAX189 12 bit ADC, 12 bit DNL Plot.

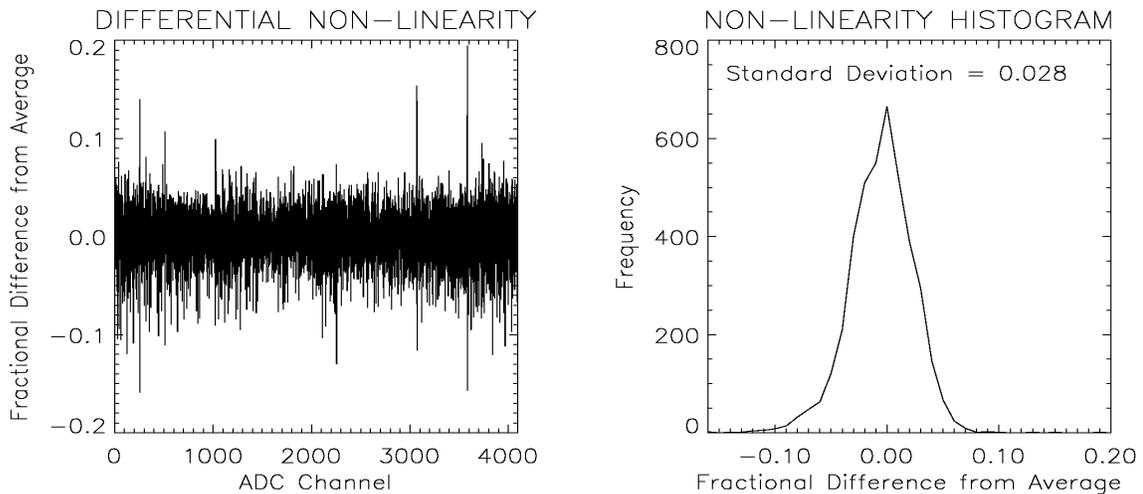


Figure 2 Maxim MAX189 12 bit ADC, 11 bit DNL Plot.

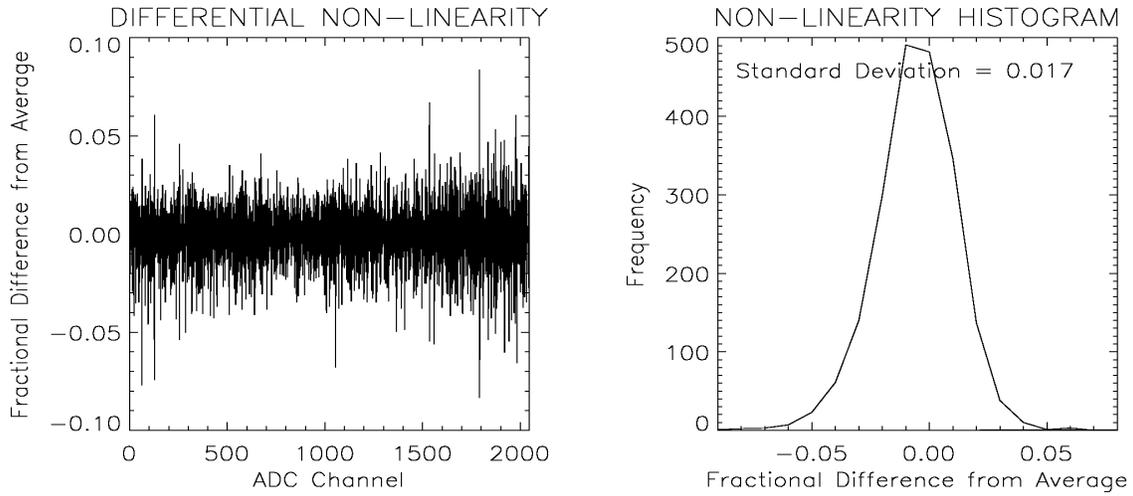


Figure 3 Maxim MAX1241 12 Bit ADC, 12 bit DNL Plot.

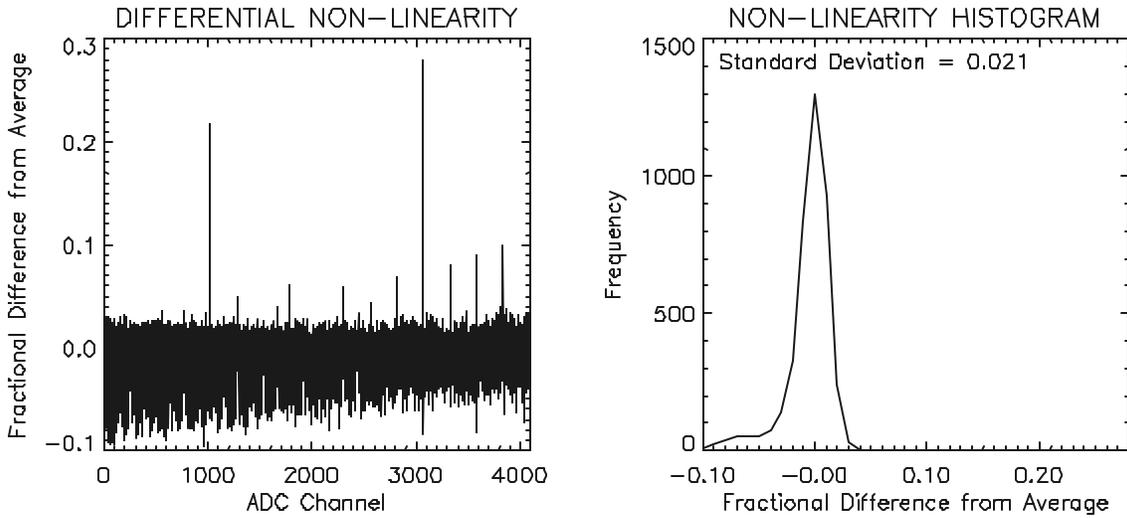


Figure 4 Maxim MAX1241 12 Bit ADC, 11 bit DNL Plot.

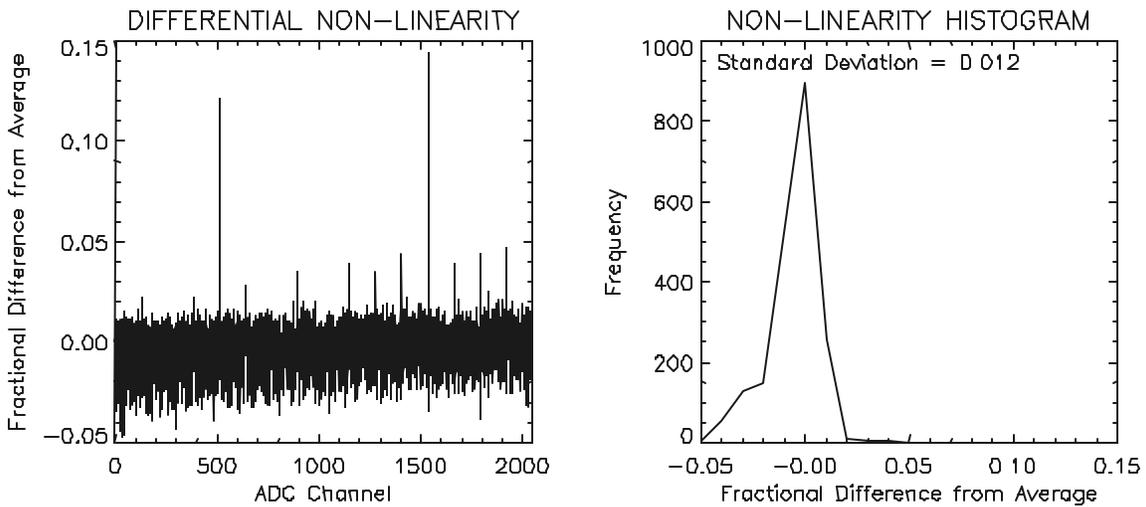


Figure 5 Maxim MAX145 12 bit ADC, Internal Conversion Clock, 12 bit DNL Plot.

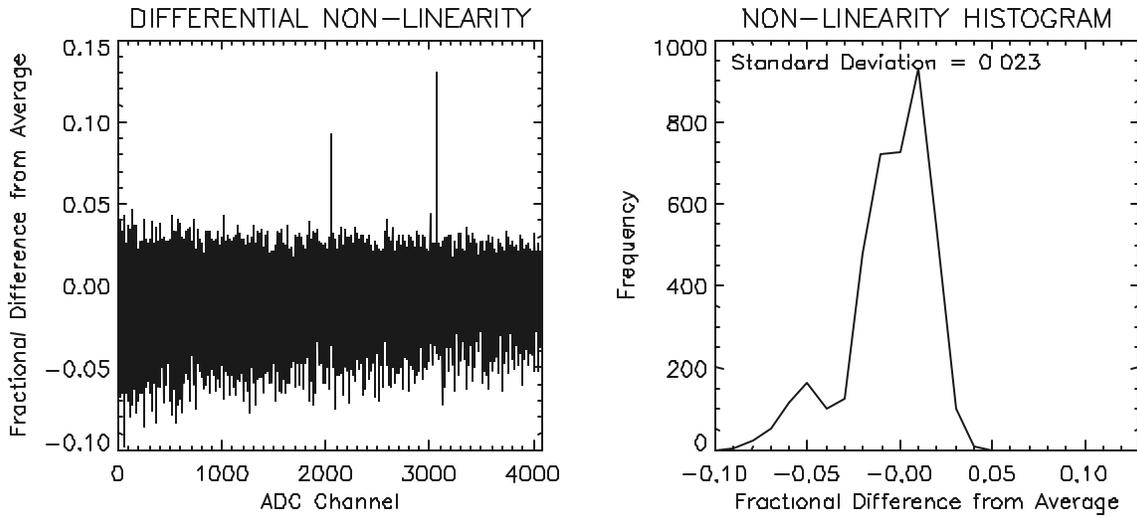


Figure 6 Maxim MAX145 12 bit ADC, Internal Conversion Clock, 11 bit DNL Plot.

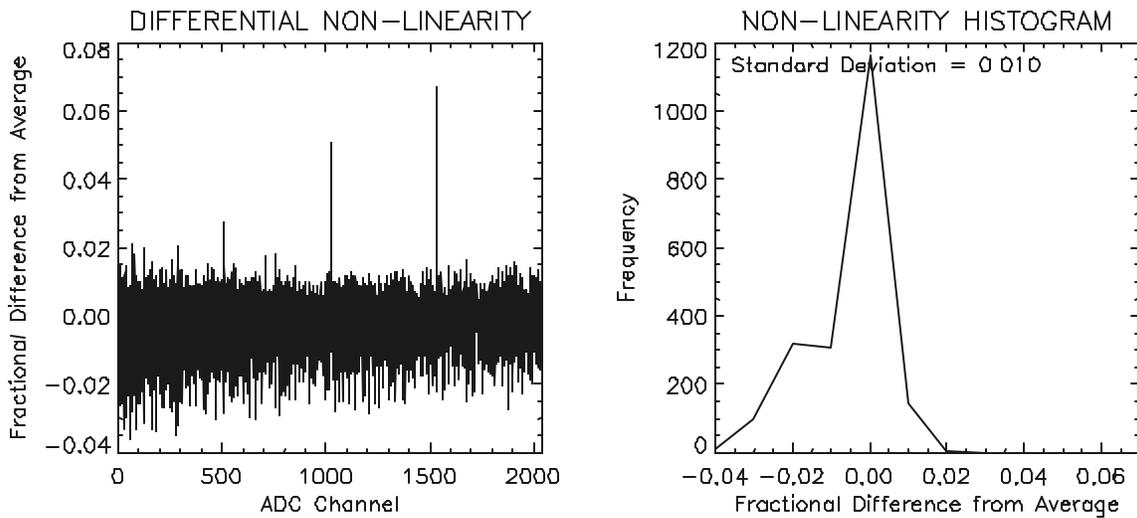


Figure 7 Maxim MAX145 12 bit ADC, 2 MHz External Conversion Clock, 12 bit DNL Plot.

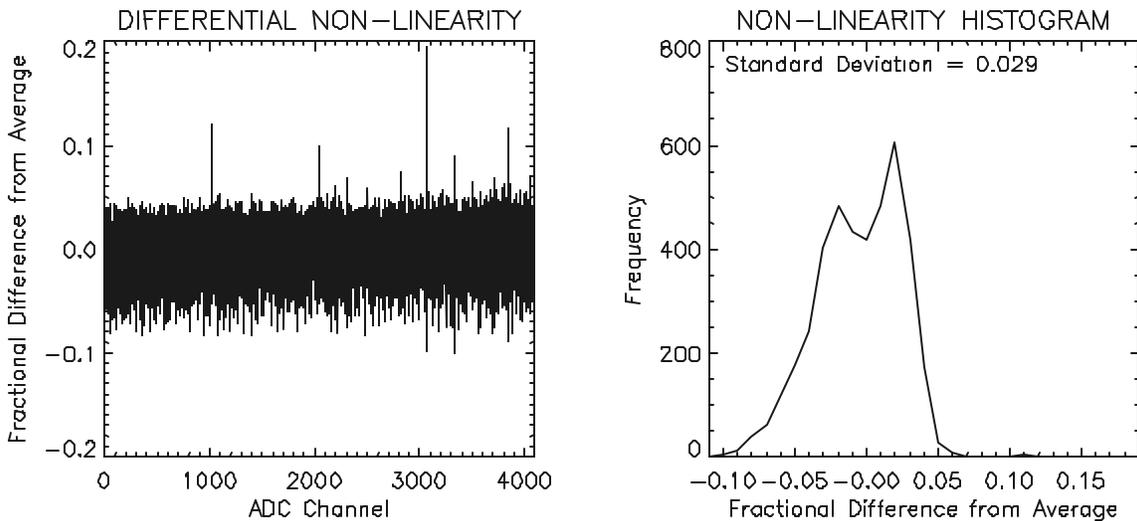


Figure 8 Maxim MAX145 12 bit ADC, 2 MHz External Conversion Clock, 11 bit DNL Plot.

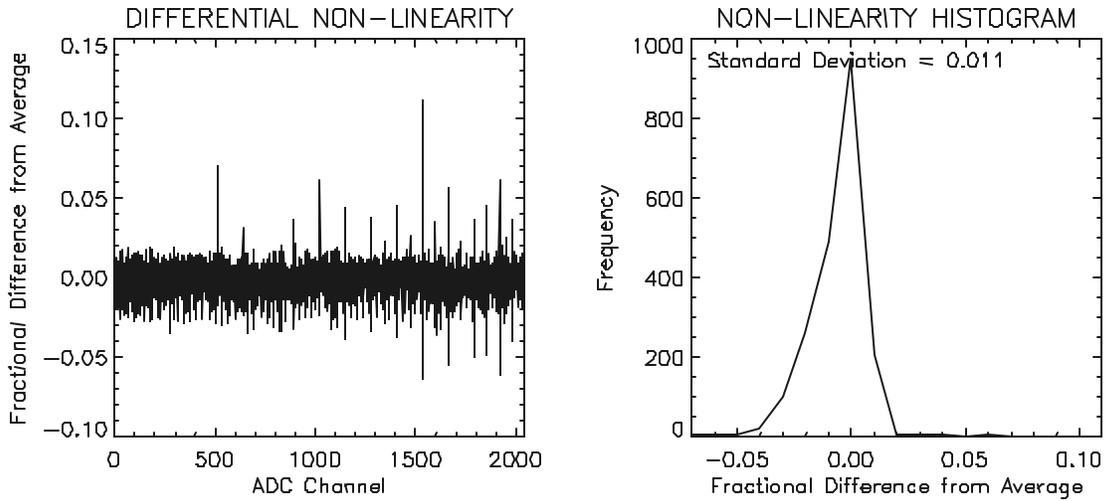


Figure 9 Maxim MAX145 12 bit ADC, 5 MHz External Conversion Clock (not spec.), 12 bit DNL Plot.

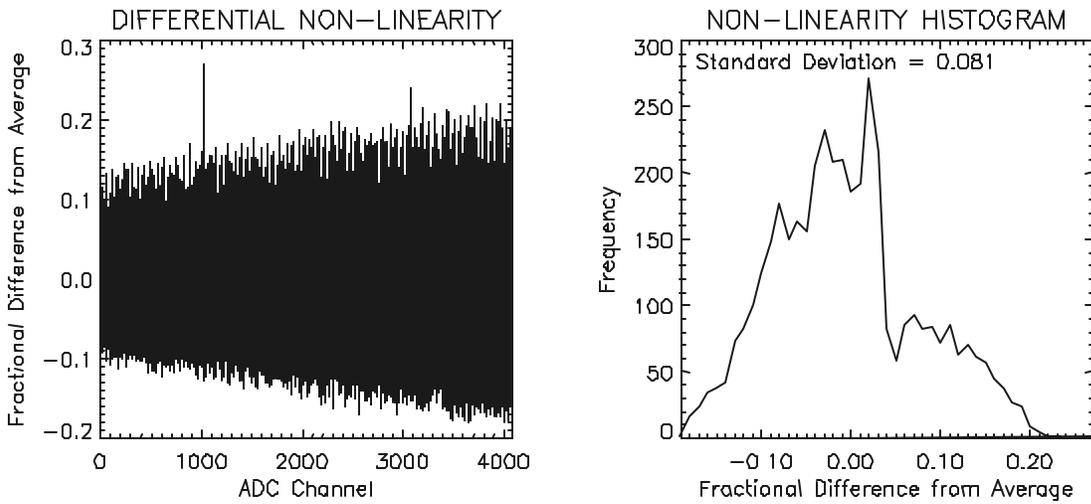


Figure 10 Maxim MAX145 12 bit ADC, 5 MHz External Conversion Clock (not spec.), 11 bit DNL Plot.

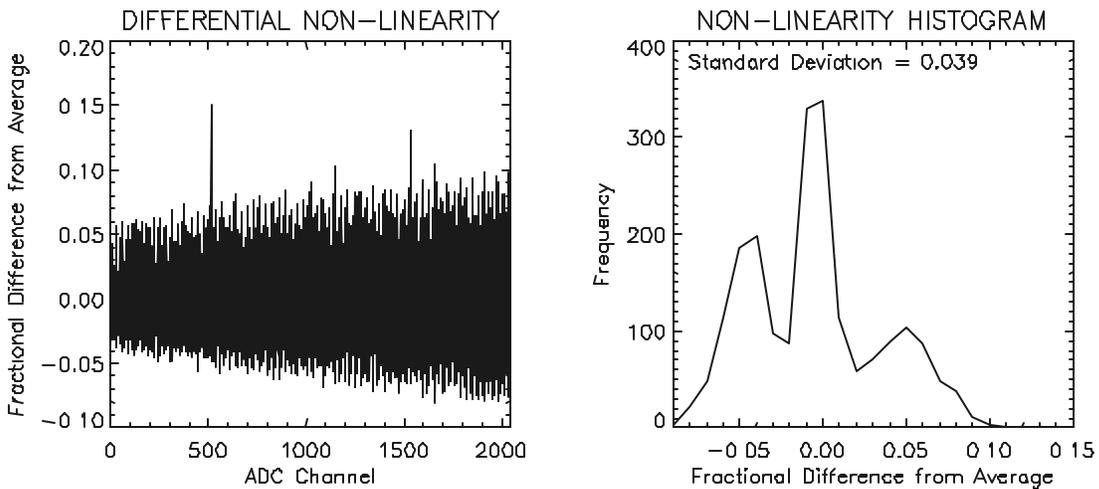


Figure 11 Burr-Brown ADS7816 12 bit ADC, 12 bit DNL Plot.

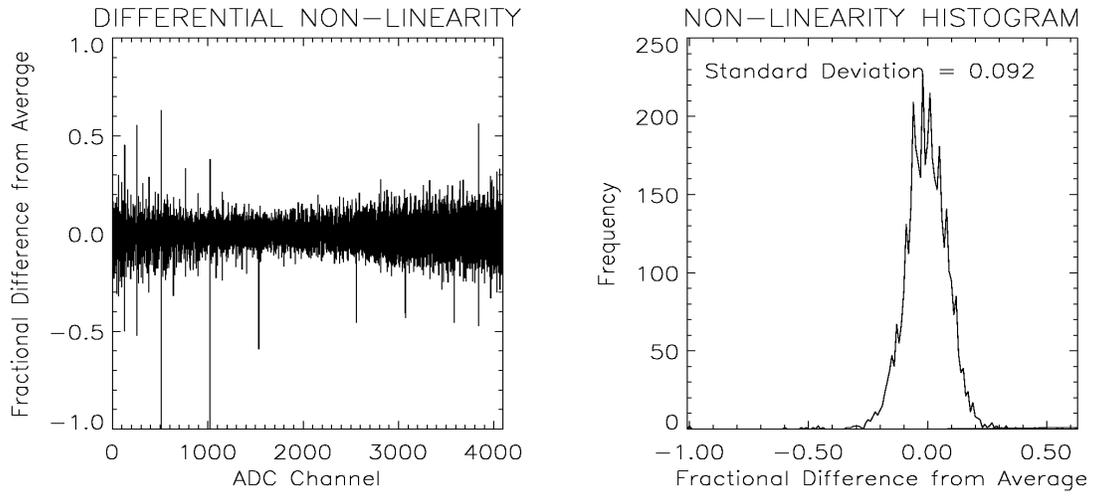


Figure 12 Burr-Brown ADS7816 12 bit ADC, 11 bit DNL Plot.

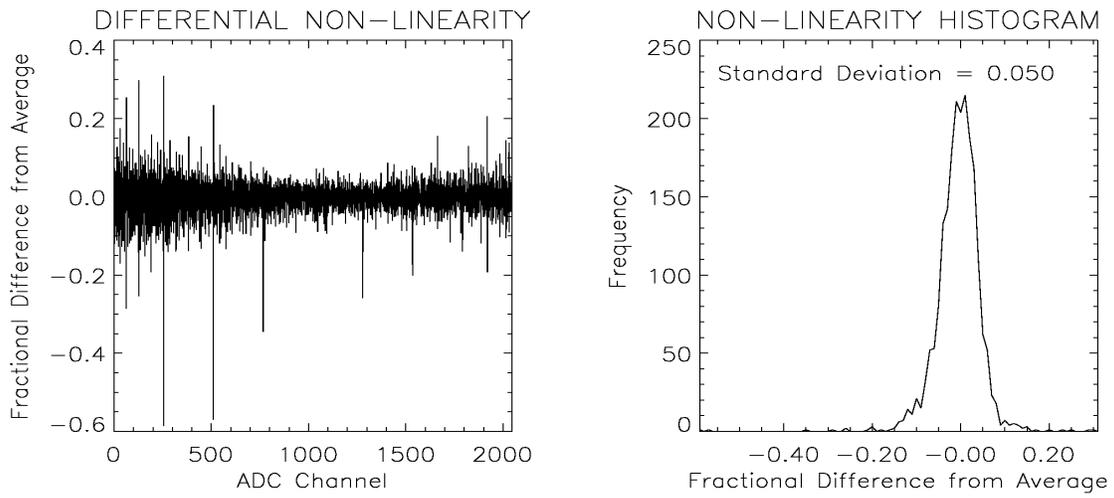


Figure 13 Analog Devices AD7475 12 bit ADC, 2 MHz Clock, 12 bit DNL Plot.

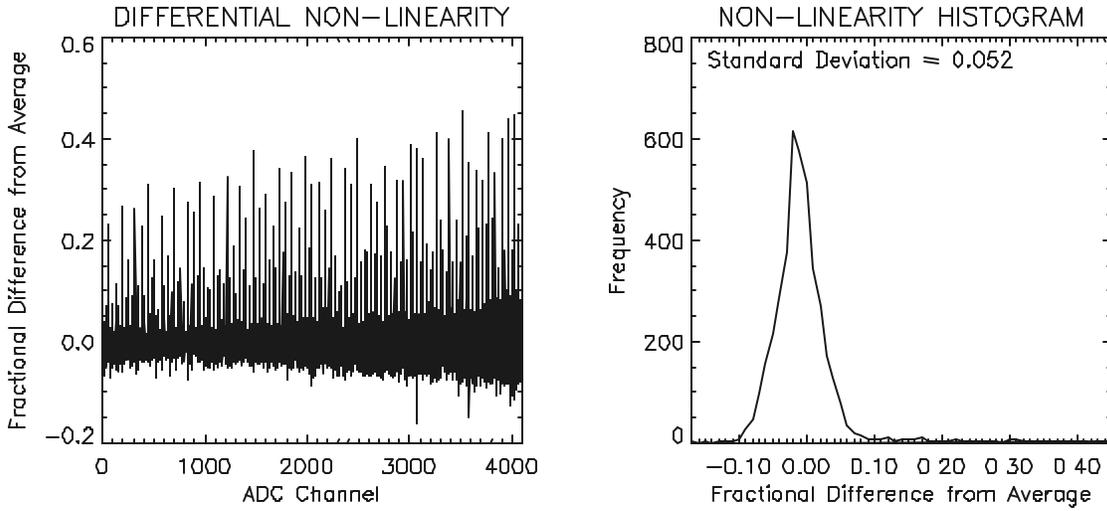


Figure 14 Analog Devices AD7475 12 bit ADC, 2 MHz Clock, 11 bit DNL Plot

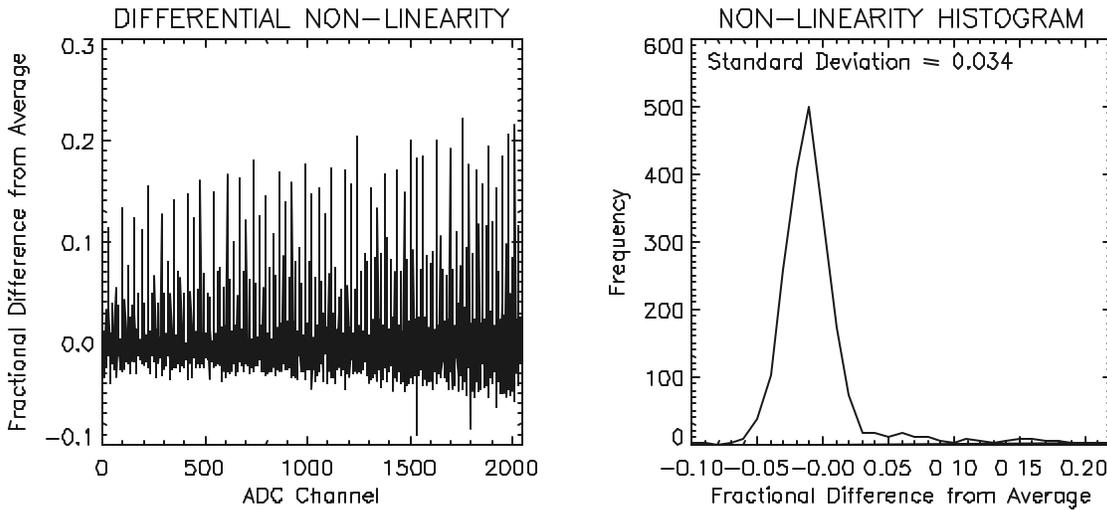


Figure 15 Analog Devices AD7475 12 bit ADC, 10 MHz Clock, 12 bit DNL Plot

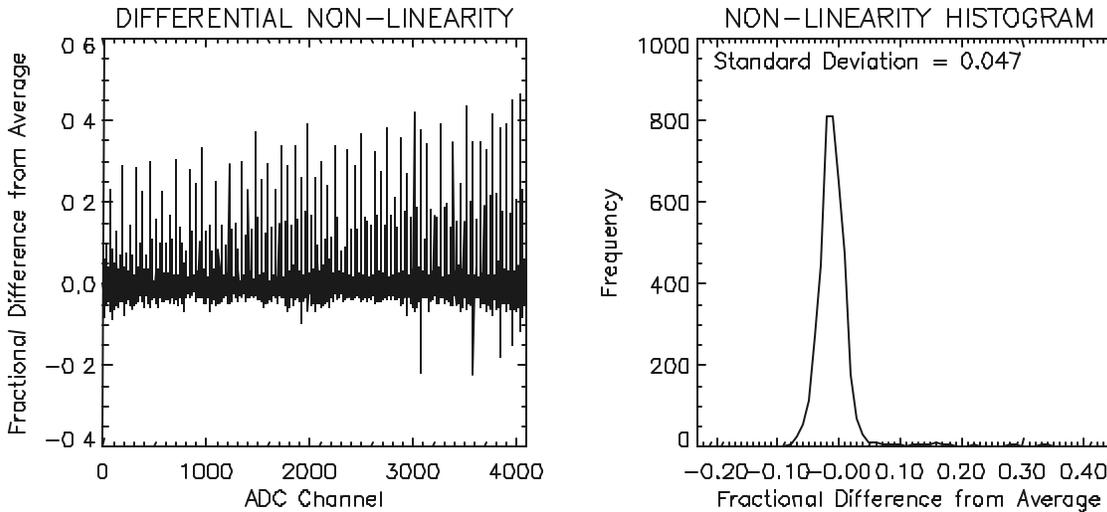


Figure 16 Analog Devices AD7475 12 bit ADC, 10 MHz Clock, 11 bit DNL Plot

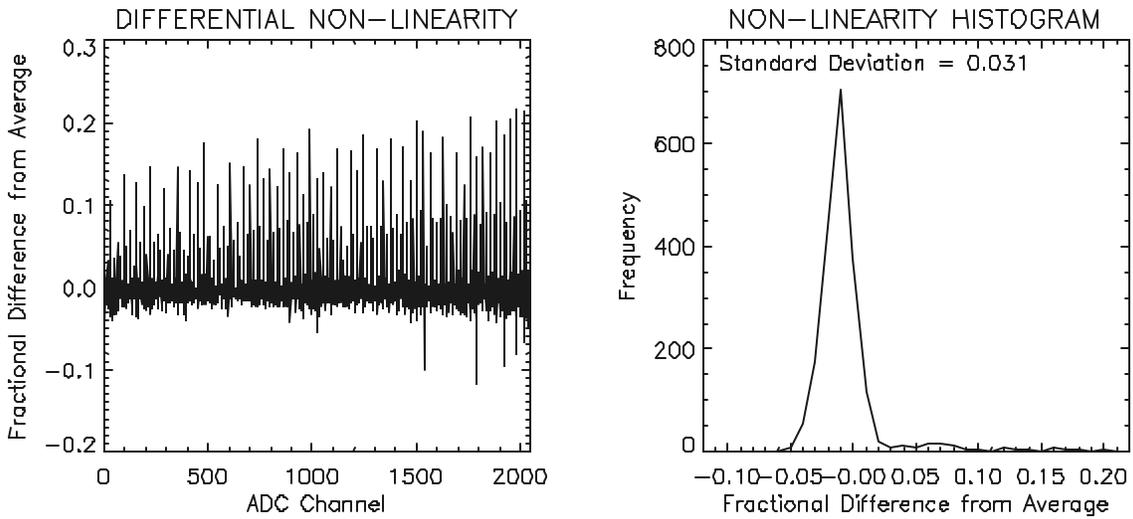


Figure 17 Analog Devices AD7475 12 bit ADC, 20 MHz Clock, 12 bit DNL Plot

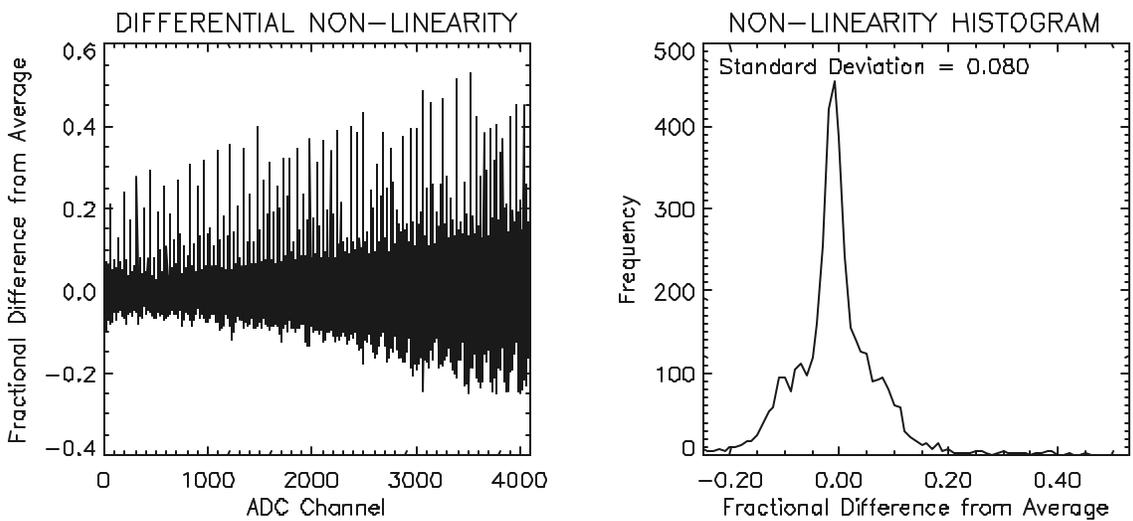


Figure 18 Analog Devices AD7475 12 bit ADC, 20 MHz Clock, 11 bit DNL Plot

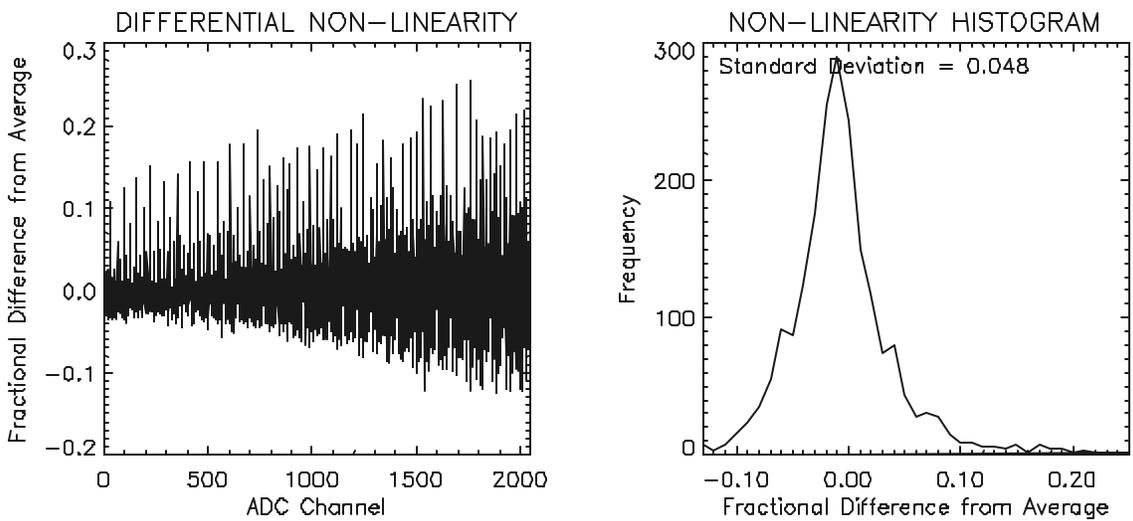


Figure 19 Burr-Brown ADS8320 16 bit ADC, 15 bit DNL Plot.

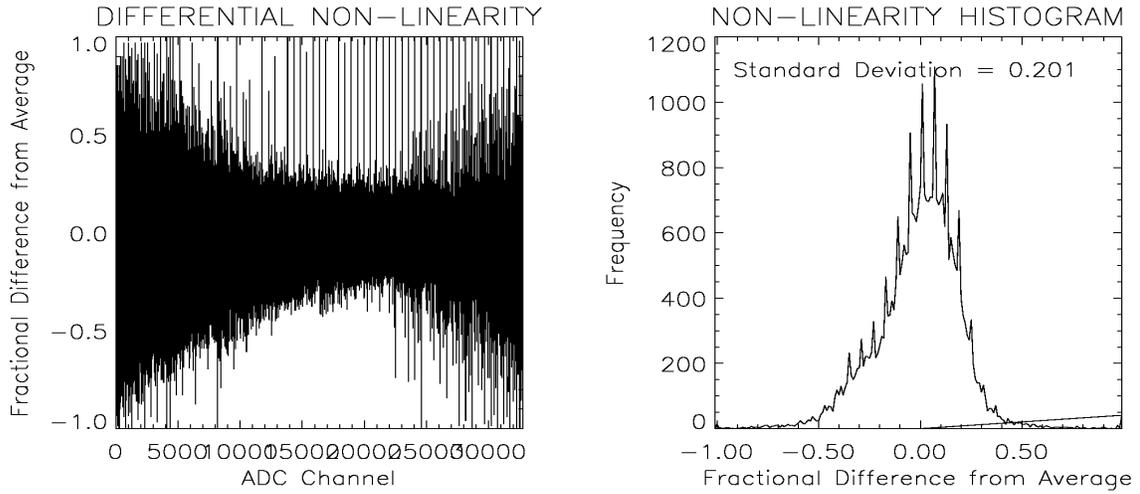


Figure 20 Burr Brown ADS8320 16 bit ADC, 14 bit DNL Plot.

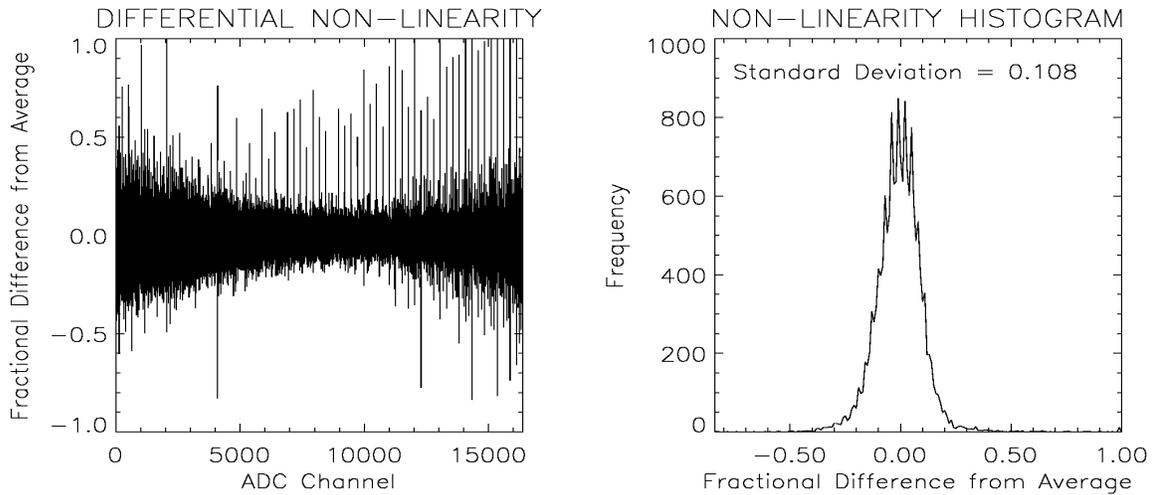


Figure 21 Burr-Brown ADS8320 16 bit ADC, 13 bit DNL Plot.

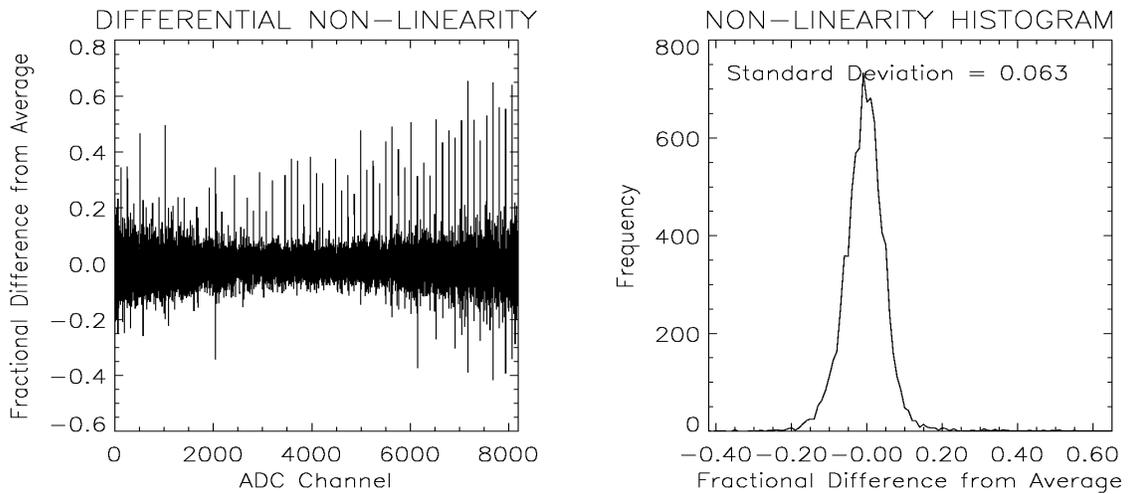


Figure 22 Burr-Brown ADS8320 16 bit ADC, 12 bit DNL Plot.

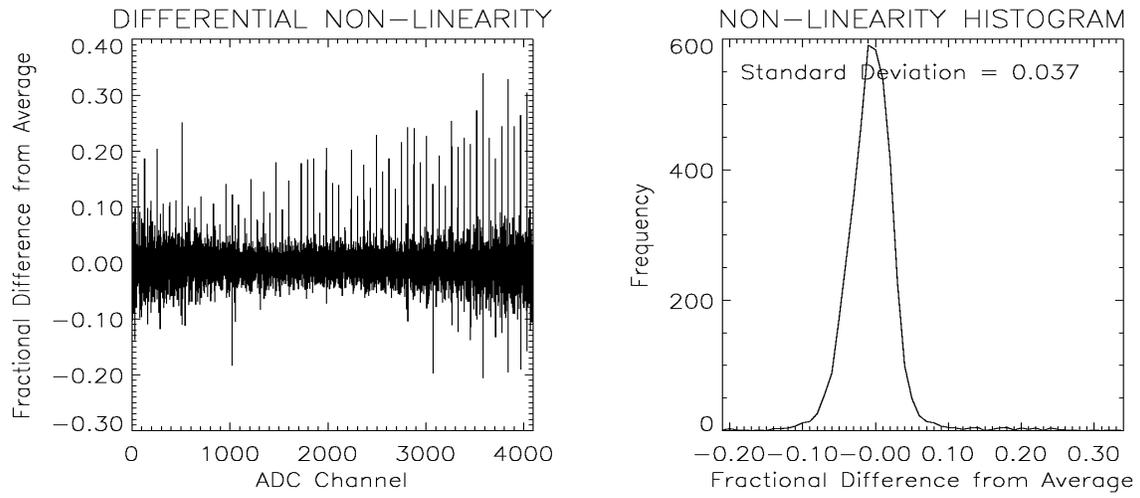


Figure 23 Burr-Brown ADS8320 16 bit ADC, 11 bit DNL Plot.

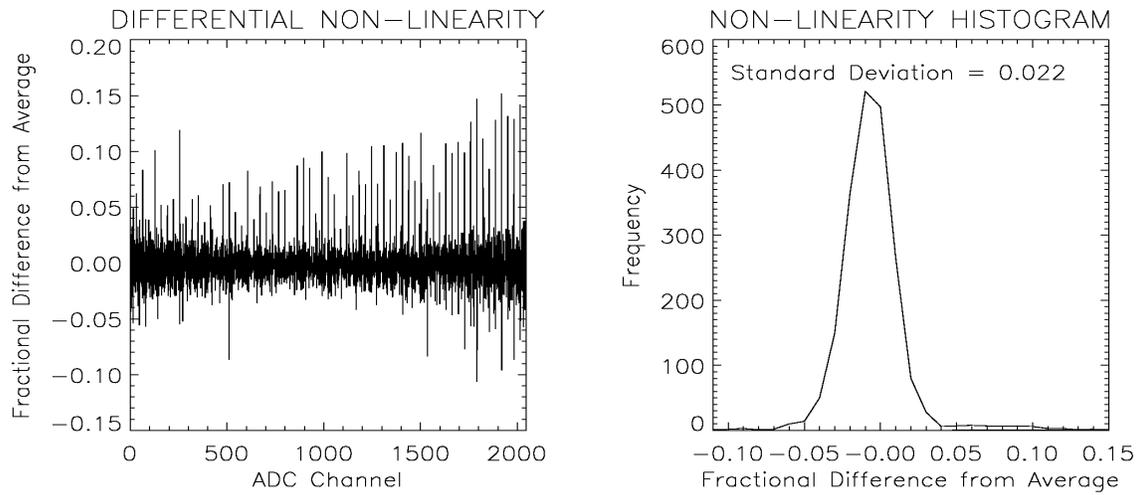


Figure 24 Maxim MAX194 14 Bit ADC, 15 bit DNL Plot.

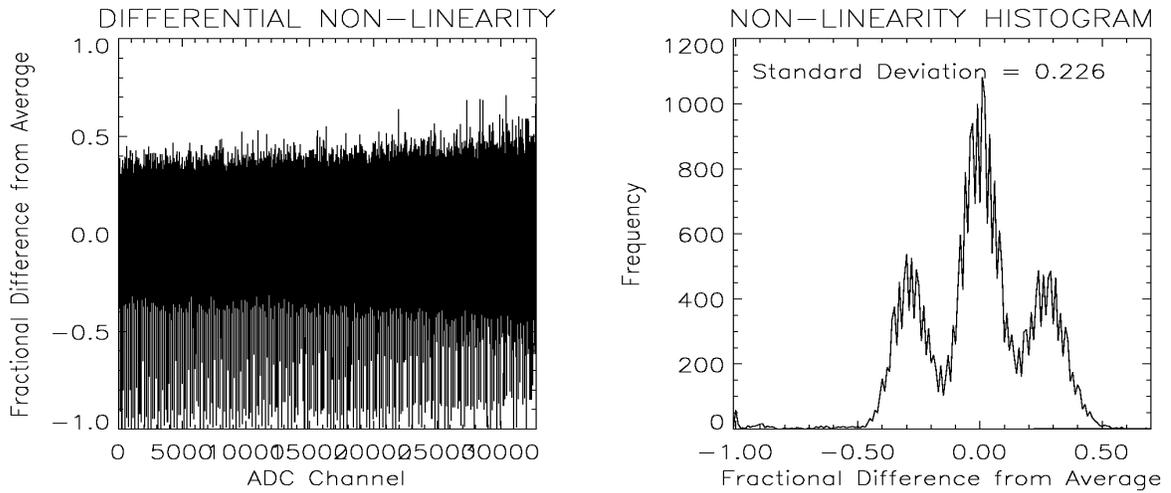


Figure 25 Maxim MAX194 14 Bit ADC, 14 bit DNL Plot.

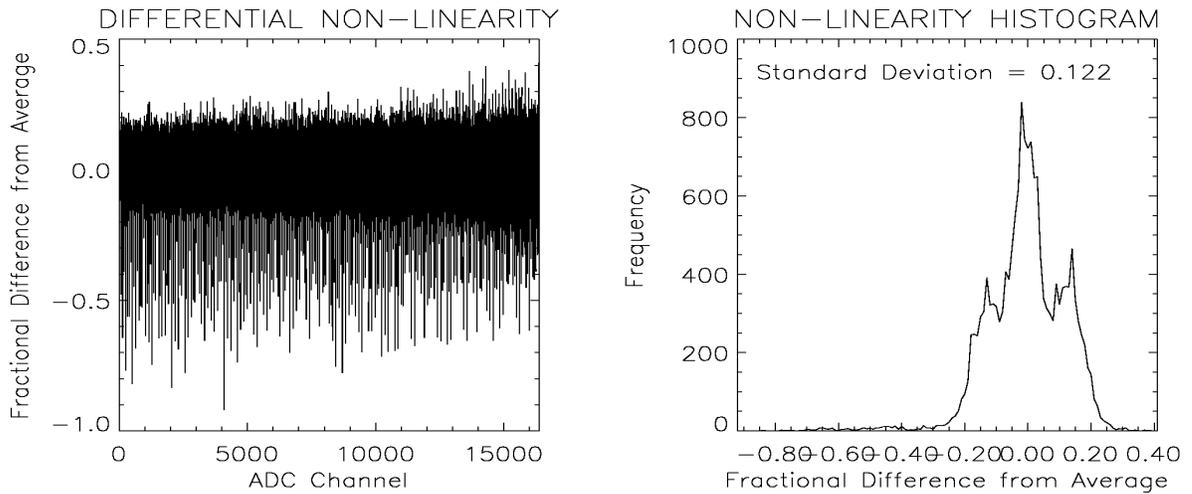


Figure 26 Maxim MAX194 14 Bit ADC, 13 bit DNL Plot.

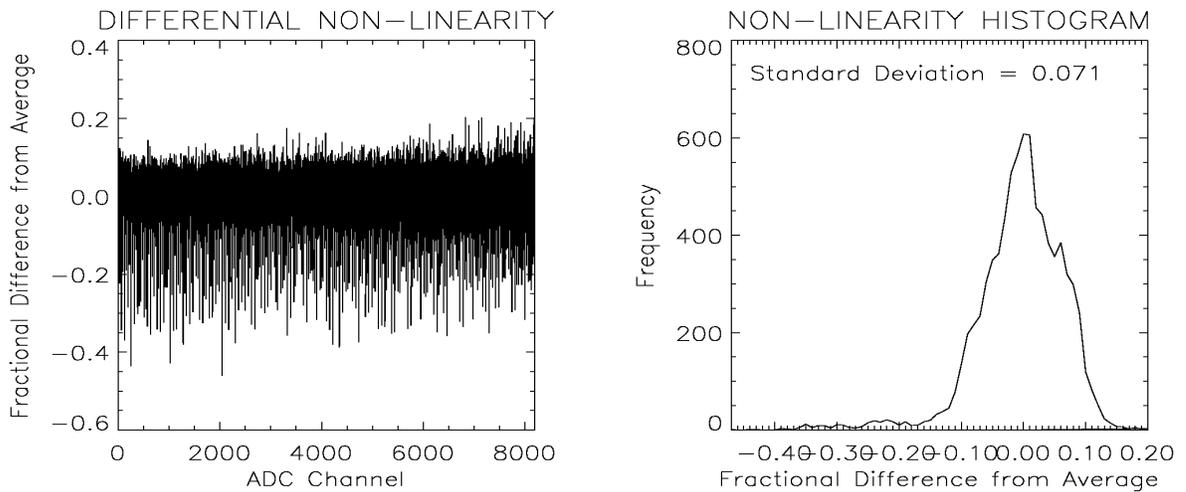


Figure 27 Maxim MAX194 14 Bit ADC, 12 bit DNL Plot.

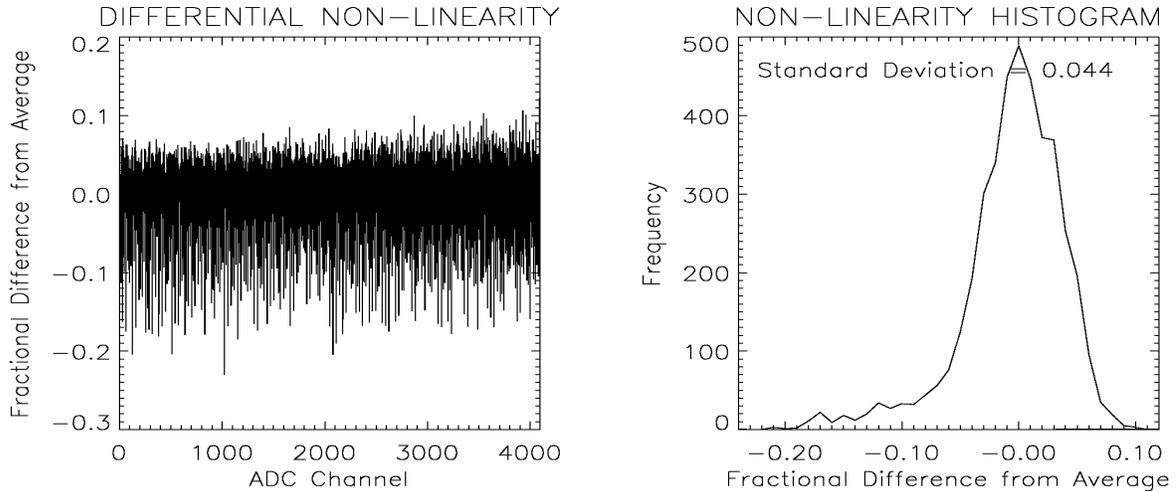
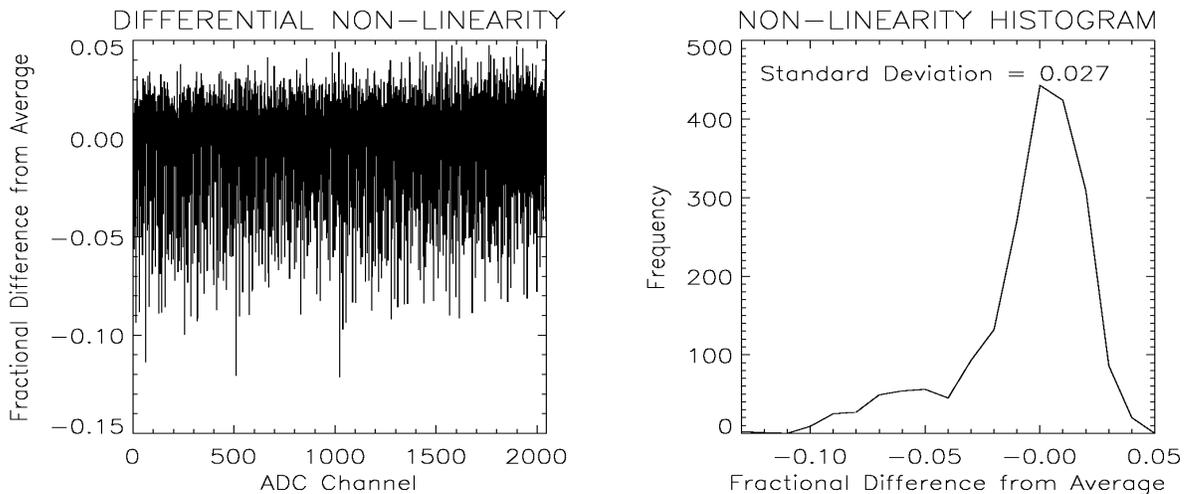


Figure 28 Maxim MAX194 14 Bit ADC, 11 bit DNL Plot.



Conclusion:

In 12 bit resolution mode, the ADC DNL standard deviations are as follows:

Table 1 ADC 12-bit resolution differential non-linearity.

Manufacturer	Part Number	ADC Resolution	12 bit Standard Deviation	Conversion Clock
Maxim	MAX189	12 bit ADC	0.028	Internal
Maxim	MAX1241	12 bit ADC	0.021	Internal
Maxim	MAX145	12 bit ADC	0.023	Internal
Maxim	MAX145	12 bit ADC	0.029	External, 2 MHz
Burr-Brown	ADS7816	12 bit ADC	0.092	External, 2 MHz
Analog Devices	AD7475	12 bit ADC	0.052	External, 2 MHz
Analog Devices	AD7475	12 bit ADC	0.047	External, 10 MHz
Analog Devices	AD7475	12 bit ADC	0.080	External, 20 MHz
Burr-Brown	ADS8320	16 bit ADC	0.037	External
Maxim	MAX194	14 bit ADC	0.044	External

The better performing ADCs are those that have internal clocks for conversion. External clocking signals can feed through the device, degrading conversion performance. The MAX194 tries to compensate for this feed through with an elaborate calibration, but is not sufficient.