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*** WBS 4.1.5 CALORIMETER (N. Johnson/Carosso)

4.1.5.1 CAL Management

Possible changes in the CAL Collaboration continue being discussed. Received preliminary proposals from French Organizations.
LAT I-PDR preparation continues.
CAL documentation update continues

4.1.5.3 Mission Assurance

- Revised contamination control plan which includes requirements for CAL, TKR and DAQ subsystems. This document was emailed for review and comments. All comments received so far are being implemented. The document will be finalized by 12/21/01.
- Revised EEE parts and electronics packaging day 2 presentation and sections related to contamination control for electronic packaging and work order database system are being deleted.
- Provided detail inputs to subsystem managers on day 2 presentations and prepared viewgraphs where required.
- Discussed critical items and parts issue with subsystem managers and designers.
- Attended ACD PDR and provided support for electronic subsystem lead for issues related to EEE parts and electronic packaging.
- Preparing handling plan for crystals.
- Preparing training plan for ESD control.
- PEM and ASIC test plans are being finalized and will be released soon.

Last week-

- Prepared CAL reliability report which includes FMEA, block diagram, probability failure rates, and critical item list.
- Prepared a cleanroom training plan for tracker and calorimeter and is being reviewed by all concerned engineers.
- Revised EEE parts plan and incorporated GSFC comments and released for official submission to GSFC through SLAC program office.
- Requested for extension of date for review of revised MAR and DIDs.
- Reviewing I&T LAT Contamination Control Plan prepared by Larry Wai and Ossie Miclican and another LAT contamination control plan prepared by Joseph Cullinan.
- Preparing presentation for PDR.
- Resolving issues related to tantalum capacitor, plastic parts, etc.

4.1.5.5 Crystal Detector Elements

Continued PIN bonding tests, thermal cycling of optical adhesives. Tenney thermal chamber is now down for installation of programmable temperature controller. Thermal cycling should resume next week. (NRL)

Continuing analysis of stability of light tapering in the 80 CsI crystals after 18 months of storage, mechanical vibration and shock, temperature cycling, humidity variation, etc etc. Analysis shows that when optical bonds degrade, the apparent light tapering decreases, presumably because of a change in reflectivity at the ends. Conducting tests now in the lab with sample crystals. (NRL)

Ecole polytechnique wrapped 12 crystals and inserted them into the LM2

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structure (quite easy job by Oscar and Alain).
Light yield on 12 crystals have been performed at the Glast /Saclay test bench (Boubou, Yves+Gilles) and LM2 has then been vibrated, (report in progress-Oscar+Alain). Visual inspection is OK. Light yield after vibration is achieved for 6 crystals, and running for the 6 others. It will be finished on Friday noon. SED made the data available on the ftp saclay site, and data analysis is in progress (Berrie). For that purpose Berrie and Xavier and Gilles were having a meeting on Monday, before Xavier left for holidays. Results will be discussed on Friday with NRL.
Hodoscope for EP test bench is being refurbished (Alain Debraine)
Intensive work done on the PIN diode bench which works now at SED.

Kapton flex specification details has still been discussed between Pierre, Jim, and Nick. Fabrication process started (Pierre).

Last week -
The chamfers made by Amcrys company do not meet specs. The issue have been discussed with NRL chiefs before their visit to Sweden. Chamfers made on 3 crystals for VM2 programme (Alain Bonnemaïson).

Light yield and wrapping :
For cross check validation before wrapping system final selection for VM2, 3 wrapped CDE have been inserted in the in the 1 layer structure (Laboratory Model) at polytechnique (Taher, Gilles, Oscar, Alain Bonnemaïson), and tested at Saclay test bench. First set of measurement and calibration achieved (Boubou, Piret, Gilles). Analyse in progress (Berrie)
Second test has been prepared. Due to meetings and time for calibration of the 24 channels only two tests will be made. This will hopefully not decrease the level of conclusions.

Test report on DPD test at Saclay shared by Boubou.
Report on the visit at SERMA written and shared by Boubou.

CDE fab and test
Meeting with Atermes company to evaluate the possibilities for industrial fabrication of CDEs (Arache, Claude, Didier Imbault, Gilles and Nick Virmani). This will be followed by a second meeting at Polytechnique (Arache organizer)

GSE
Cosmic bench mechanics has been completed at polytechnique (Alain, Michel, Taher).
Work on AFEE board (Alain)
CDE test bench in progress at Collège.

4. 1. 5. 6 Pre Electronics Module

Thermal test with Al dummies completed 14 cycles between -45 and + 85 °C. Structure disassembled for inspection. Visual inspection reveals no damage. Dimensional inspection will be performed in January, before vibration test.

4. 1. 5. 7 Analog Front End Electronics

Testing of GCFE ver 3 chip has produced linearity plots of all gain ranges and channel crosstalk plots. Non-linearity of the low amplitude signals has been attributed to the output buffer, which has been improved in the GCFE version 4 submitted last October. SLAC will be modifying their software to run crosstalk measurements as well.

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Integration of the Cal VM single row electronics to TEM Comm Card is progressing also. There is a definite noise problem of the commercial LVDS drivers signals getting corrupted by 3.3V logic signals. Temporary solution is not to route the affected LVDS signals through the AFEE board to GCRC_Sim board connector. The signals are interfering through the maximum 1 inch length, small pitch connector between the two boards. The advantage of this connector was it fit the same foot print of the flight GCRC package, 80 pin 0.5 mm pitch. The longer term solution is re-designing the Cal VMI AFEE board, socketable Xilinx GCRC_Sim board, and new additional GCRC ASIC board, using a different connector scheme. Progress of the integration of the Cal VM single row board to the TEM Comm Card has resulting in verifying the correct design of the GCRC readout bit patterns. GCFE range bits and ADC bits have been verified after being decoded from the bit stream and displayed on a computer monitor.

We have started designing a simple GCRC test board, which will apply test vectors to the GCRC ASIC and check GCRC outputs against stored results. This will be useful in testing chips under different environments and for developing the flight ASIC test vectors. We plan to design a similar, but more complicated board for the GCFE ASIC.

4. 1. E. 3 CAL Balloon Flight

Started search for CNO in balloon flight data. Trying to understand GCR fluxes and event rates. (NRL)

4. 1. D. 2. 5 LAT SW Support

Ground Software

Continuing work on definition of Digi algorithms. Analyzing SLAC97 BT data of sample crystals to test Hits concept. (NRL)

Applying new calibration algorithms/techniques to SLAC99 BT data for two reasons: (1) to test technique at a different epoch, and (2) to provide a useful calibration for Jan 00 proton data. (NRL)

Continuing participation in understanding/modeling particle environment in LEO. (NRL)

Flight software

Working on concept for additional s/w trigger for GCR calibration events to reduce the calib data rate. Reduction comes from restricting the geometry and making a crude cut on nuclear interactions. This improves efficiency of telemetering useful GCR events at the cost of added complexity in FSW. Report in progress. (NRL)

Last week-

Software and Science meeting organized at Collège by Arache. Numerous presentations and discussions during one day on simulation, reconstruction, ballon flight, crossed calibration, sciences issues, work to be organized/done ... (from participants : congratulations to Arache for this successful meeting !)