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	Prepared by(s) W. Neil Johnson, James Ampe	Supersedes None
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Document Title **Calorimeter Front End ASIC – GCFE V9 Design Description**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Design Description of the Glast Calorimeter Front-End Electronics (GCFE) ASIC

(GCFE9 submission)

DOCUMENT APPROVAL

Prepared by:

W. Neil Johnson
Naval Research Lab

Date

James Ampe
Naval Research Lab

Date

Approved by:

Gunther Haller
LAT Electronics Manager

Date

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
GCFEv8	2/7/03	Update document for GCFE ver 8. Added sections on automatic preamp reset and calibration charge injection capacitance changes. Updated figure 1 to show new gain of output buffer.
GCFREv9	4/10/03	Update document for GCFE ver 9. Included description of added buffer output amp series resistance.

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1 PURPOSE

This document describes the conceptual design for the GLAST Large Area Telescope (LAT) Calorimeter Front-end Electronics (GCFE) ASIC.

2 SCOPE

This document gives an overview over the conceptual architecture of the GLAST LAT Calorimeter Front-end Electronics (GCFE) ASIC.

3 DEFINITIONS

3.1 Acronyms

GLAST – Gamma-ray Large Area Space Telescope

GRB – Gamma-Ray Burst

LAT – Large Area Telescope

TBR – To Be Resolved

CAL – Calorimeter Detector

TRG – L1 Trigger

GLB-TRG – Global L1 Trigger

TEM – Tower Electronics Module

3.2 Definitions

μsec, μs – Microsecond, 10^{-6} second

Dead Time – Time during which the instrument does not sense and/or record gamma ray events during normal operations..

s, sec – seconds

4 APPLICABLE DOCUMENTS

Documents that are relevant to the development of the GCFE concept and its requirements include the following:

4.1 Requirement Documents

GLAST00010, “GLAST Science Requirements Document”, P.Michelson and N.Gehrels, eds., July 9, 1999.

LAT-SP-00010, “GLAST LAT Performance Specification”, August 2000

LAT-SS-00018, “LAT CAL Subsystem Specification”, January 2001

4.2 Conceptual Design Documents

[1] GLAST Calorimeter Analog Front-End ASIC Design Consideration, Neil Johnson, NRL

[2] LAT Electronics System – Conceptual Design

[3] LAT Calorimeter Electronics System

[4] LAT GCFE Specification

[5] LAT TKR-CAL Tower Electronics Module – Conceptual Design

[6] LAT Control Protocol within LAT – Conceptual Design

[7] LAT Data Protocol within LAT – Conceptual Design

[8] LAT Housekeeping within LAT – Conceptual Design

[9] LAT L1 Trigger System – Conceptual Design

5 INTRODUCTION

The *GLAST* electronics system is described in [2]. The calorimeter sub-system electronics is documented in [3]. One of the custom ASICs required is the Glast Calorimeter Front-End Electronics (GCFE) ASIC. The basic functions of the GCFE include charge-sensitive amplification, shaping, multi-range post-amplification, trigger function, track&hold function, and auto-range selection. The key challenges for the ASIC are the large dynamic range and low power dissipation as specified in [4]. Target fabrication processes for the ASIC is the 0.5 um Agilent CMOS process. The GCFE described in this document serves one crystal end.

The conceptual design in this document is based on a design documented in [1].

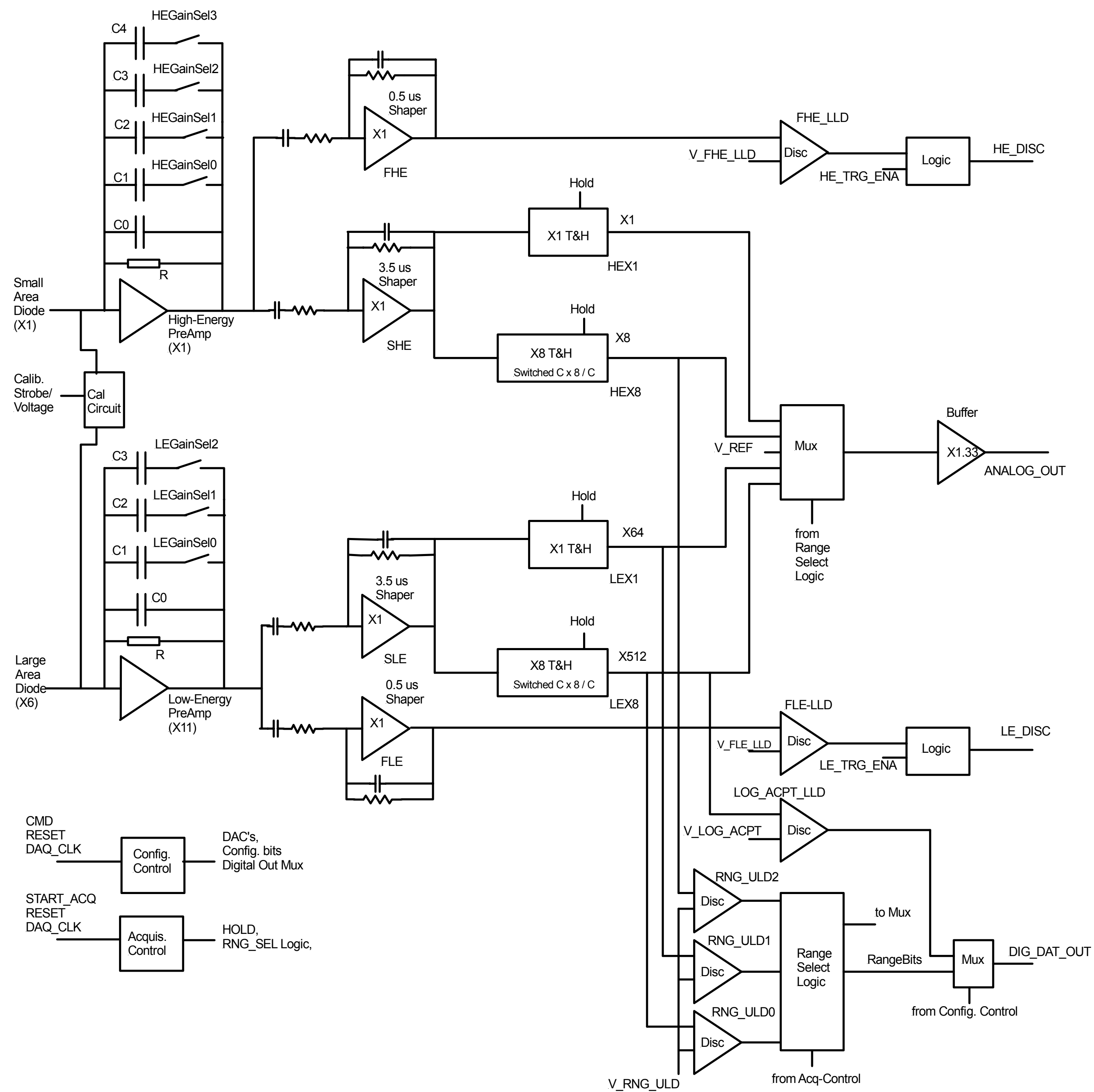

Figure 1. GCFE Block Diagram

6 GCFE Description

6.1 GCFE Overview

The ASIC amplifies signals from 2 diodes per crystal end, a large area diode covering low energy range, and a small area diode covering the high-energy range. The large area diode is four times the size of the small area diode.

The signals from the two diodes are converted into voltages by charge-sensitive preamplifiers as shown in Figure 1. The gain of the preamplifiers can be adjusted digitally. The output signal of the preamplifiers are split into two paths each: a 0.5-μsec (fast) and a 3.5-μs (= slow peaking time) shaping amplifier.

The 0.5-μsec shapers are called Fast Low-Energy (FLE) and Fast High-Energy (FHE) shapers. Those shaper outputs are compared to analog (trigger) thresholds by discriminators and sent off the IC, called LE_DISC and HE_DISC. Both trigger output signals can be disabled in the circuit via configuration bits, HE/LE_TRG_ENA. The discriminators are labeled FLE_LLD and FHE_LLD for Fast Low/High Energy Low-Level-Discriminators. The FLE_LLD and FHE_LLD threshold voltages V_FHE_LLD and V_FLE_LLD are generated on-chip by two 7-bit DACs, FHE/FLE_DAC.

The 3.5-μsec shapers are called Slow Low-Energy (SLE) and Slow High-Energy (SHE) shapers. The output of the the SHE shaper is split into two Track and Hold (T&H) stages, a times one (HEX1) and a times eight (HEX8). The output of the the SLE shaper is similarly split into two Track and Hold (T&H) stages, a times one (LEX1) and a times eight (LEX8). These T&H stages will enable the sampling of the shaper output via a HOLD signal. In normal mode the outputs will be sampled around the time of the peak. The times eight T&H stages (HEX8, LEX8) incorporate a switched capacitor stage with capacitor ratio of 8 to achieve the factor of 8 amplification. This simplifies the circuit and completely eliminates the saturation feed-back effect to the x 1 stage. Tables in the “Signal, Gain, and Noise Parameter” section show the details for the ranges. Including the ratio of the diodes, the resulting effective electronic gain ranges are x1, x8, x64, and x512.

The outputs of the T&H circuits are connected to a set of discriminators and to an analog muliplexer block. All the ranges with the exception of the highest energy (lowest electronic gain) range, HEX1, have a range-selection comparator. The HEX1 range is selected when all other ranges are in saturation. The three range-select discriminators are latched at the time the T&H circuit is put into the HOLD state, which will keep the three range-bits constant for the following range-selection block. The range-select threshold voltage V_RNG_ULD is common to all range-discriminators and generated by an on-chip RNG_ULD_DAC. Normally the threshold voltage is set to approximately 90% of the full range of the T&H output.

The range-selection block determines which of the four T&H output signals to pick and sets the analog multiplexer to output the selected range. In the auto-range mode the highest gain range not exceeding V_RNG_ULD is selected. There are additional readout modes as explained in the Range-Selection section. The selected range is decoded into two range-bits and connected to the digital output multiplexer to be sent off the IC.

The analog multiplexer is followed by an output buffer which adjusts the offset and gain to match the input range of an external ADC.

A discriminator connected to the LEX8 Track&Hold generates a log-accept signal. The latched output, LOG_ACPT, of the discriminator is used on a higher system level to decide whether to keep the channel or to discard it (“zero-suppression”) when the signal is below a programmed threshold [x]. This threshold voltage, V_LOG_ACPT, is generated on-chip via a 7-bit DAC, LOG_ACPT_DAC.

There are two control blocks shown in Figure 1. The configuration control decodes external input signals and controls the writing or read-back of on-chip registers and DAC’s. The input signals are command (CMD) carrying the GLAST serial command protocol [x], data-acquisition clock (DAQ_CLK), and reset signal (RESET). When reading back configuration data, the configuration control will take control of the digital output of the IC while sending out the requested data. At other times the digital output line is used by the data-acqusition control block.

The data-acquisition control decodes the above listed RESET and DAQ_CLK signals together with a start-acquisition (START_ACQ) signal. The circuit controls the T&H, the range-select latches, the range-selection circuit, and the transfer of the range and log-accept bits to the digital output.

The calibration block shown in Figure 1 is used to inject known signals into the preamplifier inputs to measure the transfer function of the signal channels. An external calibration voltage and strobe is applied for that purpose. The low and high energy channels can be enabled in any combination as determined by bits in the configuration register. There are two gain settings for the calibration signal to ensure performance across the entire input signal range.

6.2 Charge Amplifier

Figure 1 includes a simplified view of the charge-amplifier. There is one feed-back capacitor hard-wired between the output and input. The low energy charge amplifier has three additional feed-back capacitors that can be connected in parallel in any combination via three gain-select mode bits, resulting in eight discrete gain settings. The high energy charge amplifier has four additional feed-back capacitors that can be connected in parallel in any combination via four gain-select mode bits, resulting in sixteen discrete gain settings; however, only nine of the gain states are useful. The fourth gain select bit for the high energy range diode switches out the nominal gain capacitor to leave a small test capacitor to achieve a large gain for ground calibration. The preamplifiers for the low and high energy range differ only in the sizes of the capacitors. The gains of the two preamplifiers are set independently. The gain settings are listed in the “Signal, Gain, and Noise Parameter” section. The feed-back resistor shown in Figure 1 is implemented as a transistor which gate is connected to a dc-reference voltage. In order to achieve faster discharge of the feedback capacitors in saturation conditions, an automatic reset circuit has been added.

6.3 Charge Amplifier Automatic Reset

The charge amplifier has circuity to automatically reset the preamp feedback capacitance whenever the preamp output voltage exceeds ¼ of the full scale output range. Figure 2 shows that the presamp reset begins occuring 10 usec after the preamp output has exceeded ¼ of the full scale output range. The preamp reset continues until the preamp output has discharged above the same ¼ of full scale mark. Output triggers of the GCFE are inhibited during the preamp reset period and for approximately 25 usec following the completion of the preamp reset. There is a control bit in Configuration Register 1 to inhibit the automatic preamp reset function.

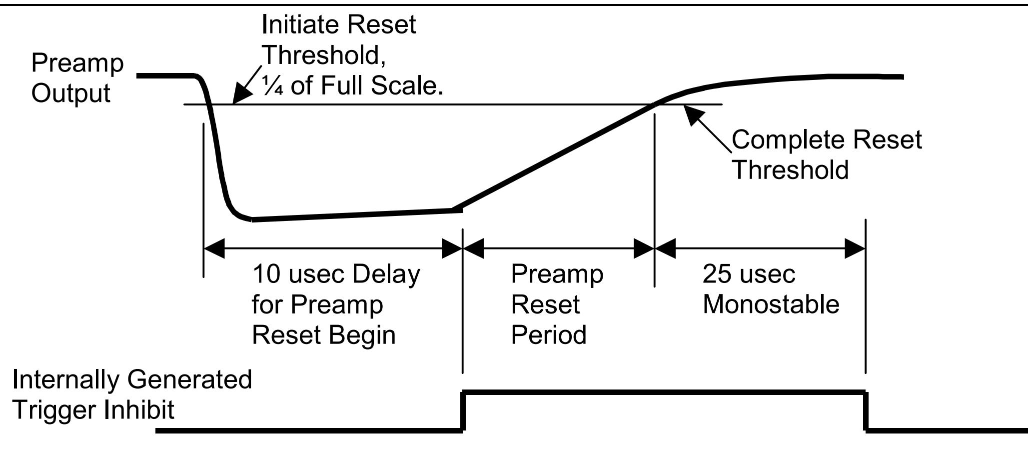

Figure 2. Automatic Preamp Reset Function.

6.4 Shaping Amplifiers

The peaking-time of the shaping amplifiers are set via internal capacitors and resistors. The shaping is single pole RC-CR with a peaking time of 0.5 μsec ($\tau_1 = \tau_2 = \sim 0.23$ μsec) for the trigger path and 3.5 μsec ($\tau_1 = \tau_2 = \sim 2.5$ μsec) for the signal path. The shaping amplifiers are AC coupled to the following post-gain stages. The fast shapers have internal, and the slow shaper have external capacitors and resistors. The slow shaper outputs are routed directly to a unity gain (x1) track and hold stage and a times 8 amplifying (x8) track and hold stage.

6.5 X1 Track and Hold

The track & hold circuit is a passive CMOS-switch – capacitor circuit followed by a high-input impedance buffer as shown in Figure 3. One control signal, HOLD, with its complement is required. The tracking time-constant is given by the resistance of the switch together with the hold capacitor (~10 ns assuming 10Kohm x 1 pF). The turn-off time of the switch is approx 1 ns. The discharge time of the capacitor via the source-drain junction of the switch in the non-conducting state is approx 100 ms (tbr). The T&H is put back into the track mode at the end of the readout cycle. A high input impedance buffer provides the drive capability for the output of the T&H.

6.6 X8 Track and Hold

The x8 gain amplifier and its T&H stage are integrated into one switched capacitor stage with a capacitor ratio of 8 as shown in Figure 4. The matching of capacitors on-chip are expected to be better than a few percent. This simplifies the circuit and completely eliminates the saturation feed-back effect to the x1 stage.

6.7 Range-Selection Discriminators

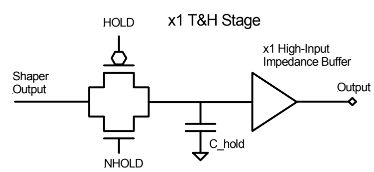

Figure 3. x1 T&H Stage

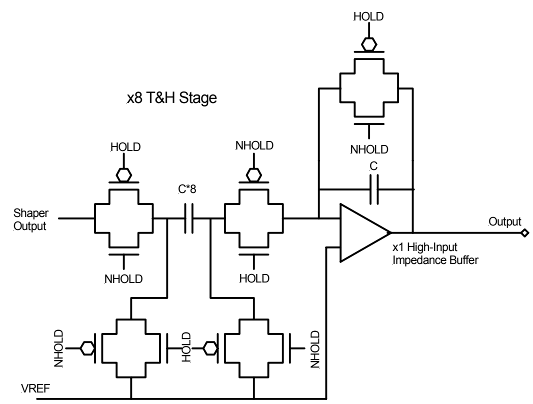

Figure 4. Integrated x8 Gain and T&H Stage

All three discriminators for the range-selection use a common 7-bit DAC voltage as threshold voltage. The threshold voltage is set to a level at which the input signal enters the non-linear region (aproximately 90% (tbr) of full-scale). The outputs of the discriminators are latched at the time the T&H is put into the HOLD state. This insures that the range-selection circuit is stable while the analog ranges are digitized. The latches are reset at the end of the readout cycle.

6.8 Log Accept Discriminator

The discriminator (LOG_ACPT_LLD) for the log accept bit compares the LEX8 T&H output signal level to a dedicated 7-bit DAC level. The output of the discriminator is placed on the output data line when the proper state machine state is reached. The discriminator output value on the data line is not latched.

6.9 Range-Selection Logic

The range selection logic determines which of the gain stages is to be connected to the analog output of the GCFE. The range-selection logic outputs 5 control lines to the analog multiplexer to connect either one of the four T&H output signals, or a DC input level generated by an on-chip DAC.

The inputs to the range-selection logic are as follows:

- RNG_ULD[2:0]: Three discriminator outputs from three gain ranges (LEX8, LEX1, and HEX8).
- FIRST_RNG[1:0]: Two First-Range bits in the configuration register which determine the first range to be selected when the Use_First_Range bit is set.
- USE_FRST_RNG: One Use_First_Range bit in the configuration register.

- OVERWRITE: One Overwrite bit in the configuration register which will continously connect the selected range to the output.
- INC_RNG: The Increment-Range signal from the signal acquisition control block.
- ENA_RNG[1:0]: Two Range-Enable bits to enable the low and high energy ranges (LEX8/X1, HEX8/X1). These bits are used to disable the ranges of the low or high energy (diode) channels in case one of the two inputs malfunctions. (Note that the enable of each of the 4 ranges individually is not needed since the likely failure is loss of one of the input (diode) connections).

Table 1 shows the relationship of the range selection control signals to the selected range for the multiplexer. In the table, the selected mux range is a function (Fct) of different input bits. The operation of these functions is described in section 8.3

6.9.1 OVERWRITE = 1

The selected range is continuously connected to the IC output, independent of any other acquisition or configuration states. The selected range depends on the USE_FRST_RNG bit.

a) If it is 0 then the DC_REF is always connected. The range bits are forced to R3.

b) If it is 1 then the range decoded from the two FIRST_RNG bits in the configuration register is connected. The range-bit reflect the range selected.

The OVERWRITE bit will enable monitoring of any of the Shaper/T&H outputs at the analog output pin of the GCFE. Note that the T&H can be continuously in tracking mode or go through the regular acquisition cycle depending on whether the START_ACQ signal is asserted or not. (e.g. during calibration). The DC_REF is a DAC, so DC tests of the signal chain from the analog multiplexer via the output-buffer through the external ADC is possible.

6.9.2 OVERWRITE = 0

Normally, between acquisition cycles, the RESET bit is asserted which results in the DC-reference voltage being selected. The DC reference from the REF_DAC is output in between acquisition cycles so that the IC output is kept constant (reduce crosstalk).

When the RESET is deasserted, then the first INC_RNG signal will select the first range.

- If the USE_FRST_RNG bit is 1, then the first range is given by the two FRST_RNG bits from the configuration register (decoding see “Range-Selection Parameters” section). This diagnostic mode enables e.g. whether the channel readout order affects the result (droops, etc). The acquisition cycle can also be aborted after the first range via the RNG_SEL_RST bit.
- If the USE_FRST_RNG bit is 0 then the first range is auto-ranged depending on the ENA_RNG bits from the configuration register and on the RNG bits from the three range comparators, see “Range-Selection Parameters” section. The second INC_RNG signal will select the next range, the order of the range. The higher-level system will cycle through all four ranges in CNO mode or abort the cycle in non-CNO mode after the 1st range. (The RNG_SEL_RST is asserted, after the 1st range, from the acquisition block in response to the RESET IC input signal). Note that the ENA_RNG bits affect only the first (auto-range) selected range. The following ranges, i.e. in CNO mode, are readout in the predetermined order ignoring the ENA_RNG bits.

Table 1. Range Selection Operating Modes

OVER-WRITE	USE_FRST_RNG	RESET	FIRST_RNG[1:0]	INC_RNG	ENA_RNG[1:0]	Range Bits [2:0]	Selected Mux Range
1	0	x	x	x	x	x	DC_REF
1	1	x	FIRST_RNG[1:0]	x	x	x	Fct(FIRST_RNG[1:0])
0	x	1	x	x	x	x	DC_REF
0	1	0	FIRST_RNG[1:0]	1st INC	x	x	Fct(FIRST_RNG[1:0])
				2nd INC		x	next range
				3rd INC		x	next range
				4th INC		x	next range
0	0	0	x	1st INC	ENA_RNG[1:0]	RNG_ULD[2:0]	Fct(RNG_ULD[2:0], ENA_RNG[1:0])
				2nd INC			next range
				3rd INC			next range
				4th INC			next range

The range-selection block outputs which of the four ranges is being selected, encoded into 2 range-bits, as listed in the "Range-Selection Parameters" section. The data-acquisition control logic puts those bits onto the digital output line of the GCFE.

6.10 Analog Multiplexer

The analog multiplexer is a five-input, one-output switch controlled by the Range-Selection Logic. Four of the inputs are from the 4 gain ranges, one from a DC reference voltage. (To ensure that the analog output of the GCFE does not change while in track mode; eliminates analog output to input crosstalk). There are 5 input control lines from the Range-Selection block.

6.11 Output Buffer

The output buffer is used to drive the load of the external ADC. It also adjusts the internal voltage range to the ADC input range. The gain of the output buffer is set to 4/3. GCFEv9 and above have a 2K ohm resistor in series with the output buffer to help isolate the buffer from the external load, and thus maintain stability of the buffer.

6.12 Trigger Discriminator and Logic

The outputs of the two 0.5 μsec shaping amplifiers (FHE and FLE) are connected to discriminators (FHE_LLD and FLE_LLD). Each discriminator has its own 7-bit DAC to adjust the threshold. The outputs of the comparators are combined with two Trigger Enable bits from the configuration register (logical AND) and connected to outputs of the GCFE, HE_DISC and LE_DISC, through a wired-or driver. The wired-or driver is a CMOS switch, which closes when the discriminator is asserted.

6.13 Trigger Rate Counter

There are no diagnostic rate counters in the GCFE. Discriminator outputs from the GCFE are processed by the GCRC and counted in the TEM.

6.14 Calibration

The GCFE receives a differential strobe and a single-ended calibration voltage. The calibration circuit can inject a charge into the inputs of both charge amplifiers. The input signal is shaped in the GCFE to approximate the input pulse from the diodes (tbr). There are two gain settings for the calibration circuit, selected by a CALIB_GAIN bit in Configuration Register 1. The low and high energy channel calibration can be enabled in any combination. The calibration enable bits, CAL_LE_ENA and CAL_HE_ENA are in Configuration Register 1. Table 2 shows the charge injection capacitance according to CALIB_GAIN selection. The larger the injection capacitance, the larger the input charge.

Table 2. Calibration Charge Injection Selections

CHANNEL	CALIB_GAIN Bit	Injection Capacitance	Comment
LE	0	11.5 pF	Autoranging Test Mode
HE	0	1.15 pF	Autoranging Test Mode
LE	1	1.19 pF	LE Gain Scale Test Mode
HE	1	11 pF	HE Gain Scale Test Mode

6.15 Configuration Control

The configuration timing is shown in Figure 5. The control block performs the following operations:

- Receives and decodes command (CMD), data-acquisition clock (DAQ_CLK) and Reset (RESET) signals.
- Loads configuration registers and DAC's.

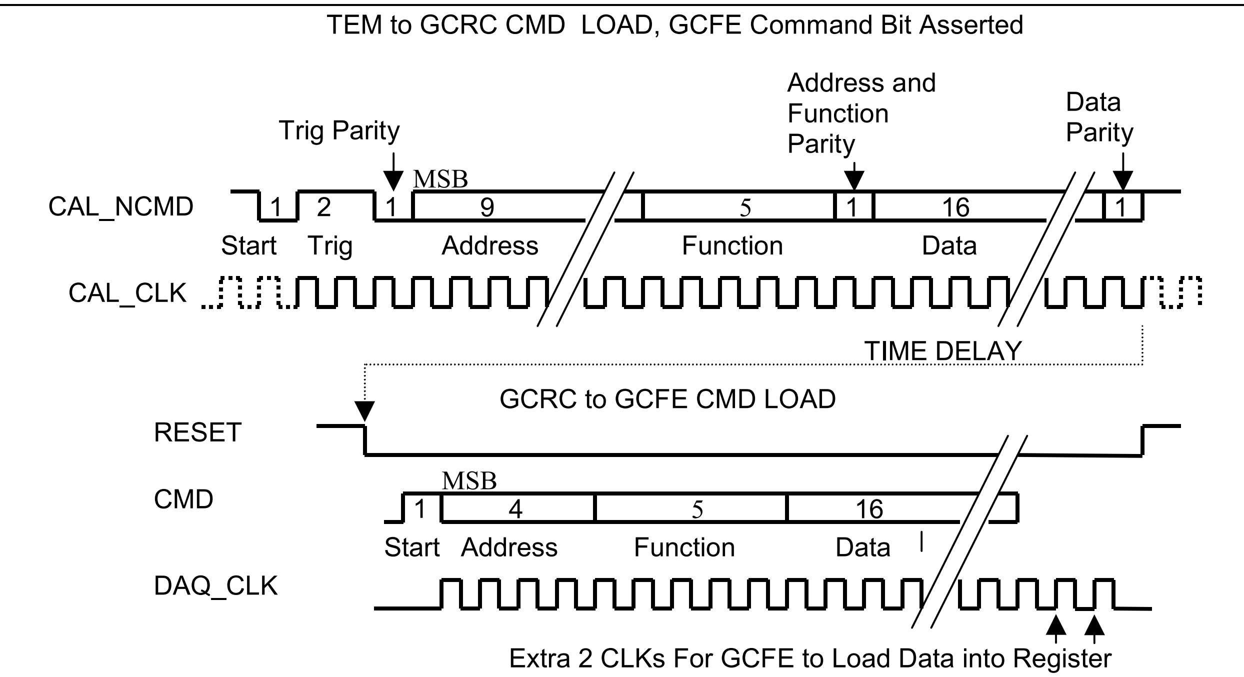

Figure 5. GCFE Command Load Timing. The top portion of the figure shows the GCRC command pattern and, in the bottom half, the resulting GCFE command pattern is shown. Note the 36 clock delay before assertion of RESET.

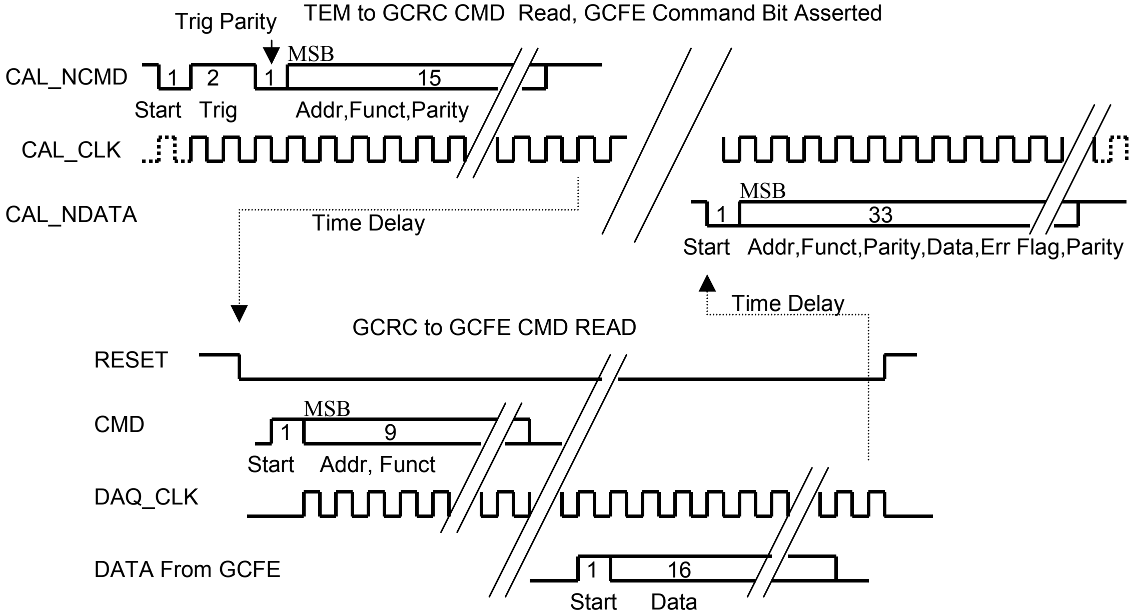

Figure 6. GCFE Command Read Timing. The GCRC receives a readback command from the TEM (top). The GCFE receive timing and response are shown on the bottom.

- Reads back configuration registers, DAC's to digital data out line. (Takes digital data output line away from the data-acquistion block during the read-back). Read back command timing is shown in Figure 6.

6.16 Signal Acquisition Control

The signal acquisition control block receives the start-acquisition (START_ACQ), data-acquisition clock (DAQ_CLK) and reset (RESET) signals. (The start-acquisition signal is generated at a higher system level from the trigger acknowledge signal, e.g. through a delay-function). The acquisition timing is shown in Figure 7. The figure shows the

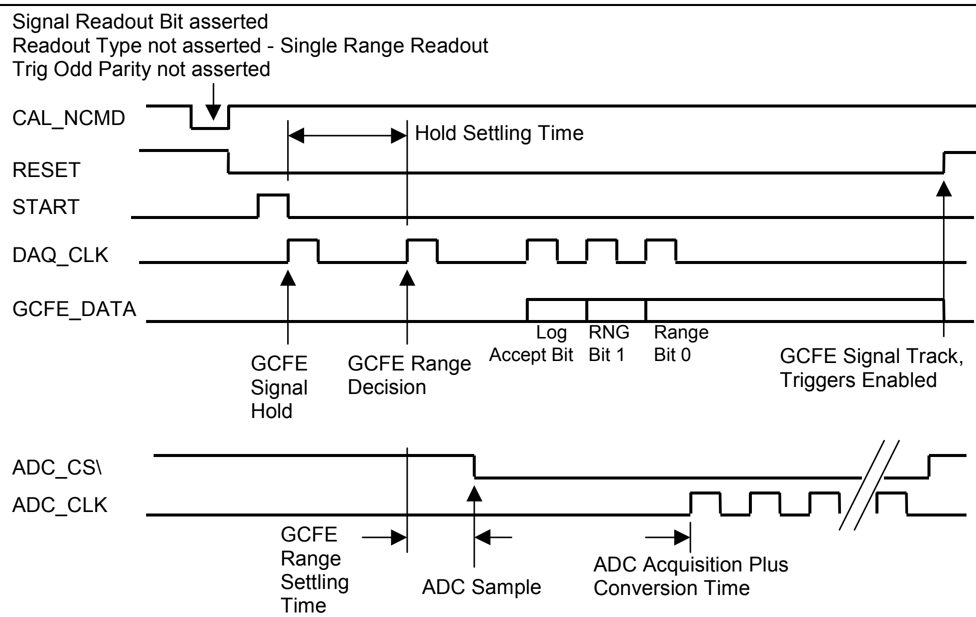

Figure 7. Signal Acquisition Timing, Single Range

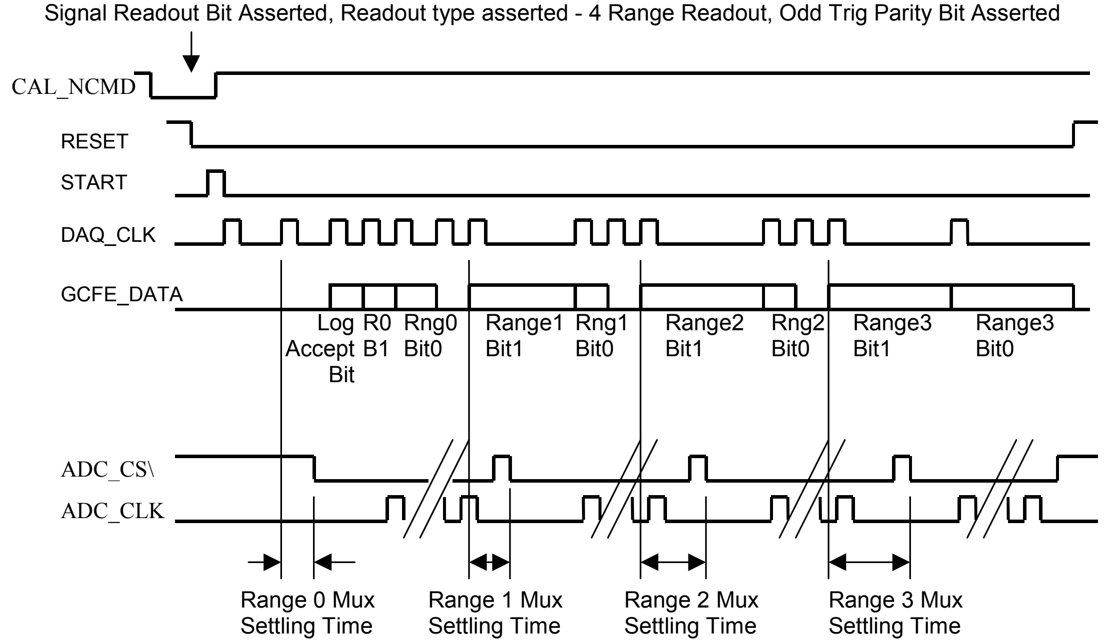

Figure 8. Signal Acquisition Timing, Four Range

sequence for acquisition of a single energy range. Figure 8 shows the timing sequence for the acquisition of all four energy ranges. The RESET and CLK signals control the number of energy ranges to be collected.

The acquisition control block performs the following operations:

- Receives the START_ACQ bit on the START_ACQ line. This starts the signal-acquisition state machine in this block.
- Generates the HOLD signal to the T&H's.
- Generates the LATCH signal to latch the discriminator outputs
- Generates the Increment-Range signal to the range-selection logic.
- RESET puts the state-machine back into the reset state, puts also the range-selection state machine back into the reset state.
- Outputs the Range-bits (RNG[1:0])and Log-Accept bit (LOG_ACCEPT) onto the digital out line of the GCFE.

7 Command Protocol

This is only a first attempt to estimate the number of commands. Content will change.

The serial command bits received on the CMD line are as follows:

- Start-bit ('1')
- 4 address bits, MSB first
- 5 function bits, MSB first
- 16 data bits, MSB first

Table 3. Command Function Bit Definitions

Funcion Bits (5 bit binary)	Meaning
00000	No op command, no action in GCFE
01xxx	write function (indicated by R = 0, D =1)
10xxx	read function (indicated by R = 1, D = 0)
RD000	Write/read CONFIG_REG_0, configuration register 0
RD001	Write/read CONFIG_REG_1, configuration register 1
RD010	Write/read FLE_DAC, low energy trigger discriminator
RD011	Write/read FHE_DAC, high energy trigger discriminator
RD100	Write/read LOG_ACPT_DAC for log accept discriminator
RD101	Write/read RNG_ULD_DAC, range-select discriminator
RD110	Write/read REF_DAC for DC reference (tbr)

7.1 Address Bits

The 4 address bits select the GCFE as set by 4 hard-wired input levels. Log 0 is “0000”. Address ‘1111’ is a broad-cast.

Note that there is one additional hardwired input bit to the GCFE, RIGHT_FIRST, which will tell the chip whether it is on the plus or minus side of the log. The address interpretation will depend on this bit (e.g. Log 0 will be Log 11, depending whether the Side-address bit is 0 or 1). This permits coordinated addressing of the two ends of a log.

7.2 Function Bits

The definitions of the functions and their 5-bit values are shown in Table 3. Note that the most significant bit of the field indicates whether the command is a write (R = 0) or a read (R = 1). Additionally, the 2nd most significant bit indicates whether the command has data (D = 1) or no data (D = 0) associated with it. For the GCFE all write commands have data; thus, they always start with “01”. All read commands for the GCFE start with “10”.

7.3 Data Bits

The data bit definitions for the two configuration registers are shown in Table 4 and Table 5. For five DAC command functions, the 7-bit DAC data field is placed in the 16-bit command data with the MSB aligned in command data bit 6 and the LSB in bit 0. Bit 0 is the LSB of the command data field.

7.4 Readback

The readback format is

- Start-bit (‘1’)
- Register or DAC bits, MSB first

The data field is always 16 bits (register/DAC bits first), may not matter (tbr). The read back is via the digital output line of the GCFE. The configuration state-machine will take control over the digital output line from the data-acquisition control state-machine while reading out.

Table 4. Configuration Register 0 (CONFIG_REG_0): Assignment of command functions

Bit Position (0 = LSB)	**Function**
0	LE_GN_SEL0: Gain_Select mode bits 0 for charge amplifier low-energy range
1	LE_GN_SEL1: Gain_Select mode bits 1 for charge amplifier low-energy range
2	LE_GN_SEL2: Gain_Select mode bits 2 for charge amplifier low-energy range
3	HE_GN_SEL0: Gain_Select mode bits 0 for charge amplifier high-energy range
4	HE_GN_SEL1: Gain_Select mode bits 1 for charge amplifier high-energy range
5	HE_GN_SEL2: Gain_Select mode bits 2 for charge amplifier high-energy range
6	HE_GN_SEL3: Gain_Select mode bits 3 for charge amplifier high-energy range
7	LE_RNG_ENA: Range_Enable bit 0 for auto-range circuit (low-energy range enable),
8	HE_RNG_ENA: Range_Enable bit 1 for auto-range circuit (high-energy range enable)
9	USE_FRST_RNG: Use first range for range selection circuit, given by First_Range bits
10	FIRST_RNG0: First_Range bit 0 for range-selection circuit
11	FIRST_RNG1: First_Range bit 1 for range-selection circuit
12	OVERWRITE: Overwrite bit (1) for range-selection circuit
13 – 15	No assignment (TBR)

8 Range Selection Parameters

8.1 Range Definition

Table 6 defines the range selection definitions for FRST_RNG[1:0] to be used when USE_FRST_RNG = 1

Table 5. Configuration Register 1: Assignment of command functions

Bit Position (0 = LSB)	Function
0	PREAMP_AUTO_RESET_ENA: Enable bit for Preamp to automatically reset for large input pulses. Bit set to 1 enables automatic preamp reset.
1	LE_TRG_ENA: Trigger_Enable for LE trigger circuits
2	HE_TRG_ENA: Trigger_Enable for HE trigger circuits
3	CALIB_GAIN: Calibration_Gain bit (1) for calibration circuit . Bit set to 0 for autoranging test.
4	CALIB_LE_EN: Calibration_Enable for low-energy calibration circuit
5	CALIB_HE_EN: Calibration_Enable for high-energy calibration circuit
6 – 15	No assignment (TBR)

Table 6. Range Definitions and Selection Order

Range	FRST_RNG1	FRST_RNG0	First Range Selected	Energy	Electronic Gain
R0	0	0	LEX8	low	high
R1	0	1	LEX1		
R2	1	0	HEX8		
R3	1	1	HEX1	high	low

The order of the ranges in the four-range readout out is:

If Present_Range <3 then Next_Range = Present_Range + 1

If Present_Range = 3 then Next_Range = 0

8.2 Range-Bit Definition

Table 7 defines the state of the two range output bits, RNG1 and RNG0, which define the selected range.

Table 7. Definition of the output range identification bits, RNG1, RNG0.

OVERWRITE	Internal Range Bits	Range	RNG1	RNG0	Range Selected	Energy	Electronic Gain
x	RangeSel0=1	R0	0	0	LEX8	lowest	highest
x	RangeSel1=1	R1	0	1	LEX1		
x	RangeSel2=1	R2	1	0	HEX8		
0	RangeSel3=1	R3	1	1	HEX1	highest	lowest
1	RangeSel4=1	R3	1	1	DCREF	N/A	N/A

8.3 Auto-Range Selection

Table 8 defines the first range selected in auto ranging mode based on the enabled ranges (ENA_RNG[1:0]) and the state of three range discriminators (RNG_ULD[2:0]).

Table 8. Auto range selection definition from range enables and discriminators.

ENA_RNG1	ENA_RNG0	RNG_ULD2	RNG_ULD1	RNG_ULD0	Auto-range Selected
0	0				**No Ranges Enabled**
		x	x	x	DC_REF
0	1				**Only Low Energy Ranges Enabled**
		x	x	0	R0 (ok, uld1 should be 0 as well)
		x	x	1	R1 (ok)
1	0				**Only High Energy Ranges Enabled**
		0	x	x	R2 (ok)
		1	x	x	R3 (ok, or could be saturated if signal is too large)
1	1				**All Energy Ranges Enabled**
		0	0	0	R0 (ok, uld1 and 2 should be 0 as well)
		0	0	1	R1 (ok, uld2 should be 0 as well)
		0	1	x	R2 (ok)
		1	x	x	R3 (ok, or could be saturated if signal is too large)

9 Signal, Gain, and Noise Parameters

9.1 Charge Amplifier Input Connection

The inputs to the charge amplifiers AC coupled to PIN photodiodes. The characteristics of these diodes are summarized in Table 9.

9.2 Charge Amplifier Low Energy Gain Ranges

Table 10 defines the gains of the low energy charge amplifier as a function of the gain selection switches LE_GN_SEL[2:0]. The nominal gain of the system is switch state 5. The ratios of the capacitors in the gain selection array are also shown in the table. Actual values of the capacitors have been estimated in the table by computing a 1.5 volt output signal from the preamp for the maximum energy deposition (Emax). The nominal capacitance uncertainty shall be less than 5% (TBR).

Table 9. Characteristics of the PIN Photodiodes

Diode	Area	Cap	Leakage @ 25 °C	Signal
Low Energy	150 mm^2	<100 pF	<10 nA	5,000 e/MeV
High Energy	25 mm^2	<15 pF	<3 nA	800 e/MeV

Table 10. Low Energy Charge Amplifier Gain Selections

Light Yield	**5000**	**e-/MeV**	**0.8**	**fC/MeV**
Emax	**1,600**	**MeV**	**1280**	**fC**
Nominal Max Voltage	**1,500**	**mV**		
Nominal Capacitance:	**853**	**fF**		
Nominal Ratio	**1.850**			

Cap Ratios **Cap Val (fF)** **STATE**	**LE_C3** 1.000 470 **LE_GN_SEL2**	**LE_C2** 0.500 240 **LE_GN_SEL1**	**LE_C1** 0.250 120 **LE_GN_SEL0**	**LE_C0** 0.600 290		**Total** **C (fF)**	**C/CNom**	**V = Q/C** **(Volts)**
0	0	0	0	1		290	0.34	4.41
1	0	0	1	1		410	0.48	3.12
2	0	1	0	1		530	0.62	2.42
3	0	1	1	1		650	0.76	1.97
4	1	0	0	1		760	0.89	1.68
5	1	0	1	1		880	1.03	1.45
6	1	1	0	1		1000	1.17	1.28
7	1	1	1	1		1120	1.31	1.14

Table 11. Low Energy Range Post-Gain Stage Characteristics

Low Energy Range Processing Range (Large PIN)	2 – 1600 MeV
LEX8 Range (3.5 μsec peaking) Calibration Threshold: Upper Limit: Noise Goal:	 2 MeV 200 MeV 0.4 MeV (2000 e-)
LEX1 range (3.5 μsec peaking) Calibration Threshold: Upper Limit:	 5 MeV 1.6 GeV
FLE Range (0.5 μsec peaking) Threshold: Upper Limit:	 5 MeV 400 MeV

9.3 Charge Amplifier High Energy Gain Ranges

Table 13 defines the gains of the high energy charge amplifier as a function of the gain selection switches HE_GAIN_SEL[3:0]. The nominal gain of the system is switch state 13. The ratios of the capacitors in the gain selection array are also shown in the table. Actual values of the capacitors have been estimated in the table by computing a 1.5 volt output signal from the preamp for the maximum energy deposition (Emax). The most significant gain selection bit, HE_GAIN_SEL3, switches to a high gain mode for ground testing.

The nominal characteristics of the low energy range post-gain stage signals are defined in Table 11.

The nominal characteristics of the high energy range post-gain stage signals are defined in Table 12.

Table 13. High Energy Charge Amplifier Gain Selections

Nominal Gain State:	**13**			
Light Yield	**800**	**e-/MeV**	**0.128**	**fC/MeV**
Emax	**100,000**	**MeV**	**12800**	**fC**
Nominal Max Voltage	**1,500**	**mV**		
Nominal Capacitance:	**8.5**	**pF**		
Nominal Ratio	**1.425**			

STATE	**HE_C4** **HE_GN_SEL3**	**HE_C3** **HE_GN_SEL2**	**HE_C2** **HE_GN_SEL1**	**HE_C1** **HE_GN_SEL0**	**HE_C0**	**Total C (pF)**	**C/CNom**	**V = Q/C (Volts)**
Cap Ratios	0.438	1.000	0.500	0.250	0.175			
Cap Val (pF)	2.10	4.80	2.40	1.20	0.84			
0	0	0	0	0	1	0.84	0.10	15.24
1	0	0	0	1	1	2.04	0.24	6.27
2	0	0	1	0	1	3.24	0.38	3.95
3	0	0	1	1	1	4.44	0.52	2.88
4	0	1	0	0	1	5.64	0.66	2.27
5	0	1	0	1	1	6.84	0.80	1.87
6	0	1	1	0	1	8.04	0.94	1.59
7	0	1	1	1	1	9.24	1.08	1.39
8	1	0	0	0	1	2.94	0.34	4.35
9	1	0	0	1	1	4.14	0.49	3.09
10	1	0	1	0	1	5.34	0.63	2.40
11	1	0	1	1	1	6.54	0.77	1.96
12	1	1	0	0	1	7.74	0.91	1.65
13	1	1	0	1	1	8.94	1.05	1.43
14	1	1	1	0	1	10.14	1.19	1.26
15	1	1	1	1	1	11.34	1.33	1.13

Nominal Operating States are 8 – 15. State 0 is test gain mode.

Table 12. High Energy Range Post-Gain Stage Characteristics

High Energy Range Processing Range (Small PIN)	100 MeV – 100 GeV 7 MeV – 7 GeV, (in test gain)
HEX8 Range (3.5 usec peaking)	
Nominal Threshold: (FOR WHAT)	100 MeV
Upper Limit:	12.8 GeV
Noise Goal:	2.5 MeV (2,000 e-)
HEX1 range (3.5 usec peaking)	
Calibration Threshold: (FOR WHAT)	300 MeV
Upper Limit:	100 GeV
FHE Range (0.5 usec peaking)	
Threshold:	500 MeV
Upper Limit:	100 GeV

9.4 Shaping Amplifier Gains

9.4.1 Fast or Trigger Shaping Amplifiers

The fast shaping amplifiers for the GCFE triggering discriminators utilize CR-RC shaping with equal time constants of 0.23 μsec in the version 5 GCFE. This provides, in simulations, a peaking time of ~0.8 μsec with CsI light yield time constants. The gain ratio for the fast shaper (the ratio of coupling to integrating capacitors) is 5.2. This gain factor, when coupled with the ballistic deficit produces a full-scale output of 2.5V at nominal gains with energy depositions of 1.6 GeV (1.5V max from the preamp) in the low range or 100 GeV in the high range. The nominal operating range of the fast shaper is from 0.100 V ("pedestal") to 2.5 Volts.

9.4.2 Slow or Signal Shaping Amplifiers

The slow shaping amplifiers for the GCFE signal amplitude digitization utilize CR-RC shaping with equal time constants of 2.6 μsec in the version 5 GCFE. This provides, in simulations, a peaking time of ~4.1 μsec with CsI light yield-time constants. The gain ratio for the slow shaper (the ratio of coupling to integrating capacitors) is 14.2. This gain factor, when coupled with the ballistic deficit produces a full-scale output of 2.5V at nominal gains with energy depositions of 1.6 GeV (1.5V max from the preamp) in the low range or 100 GeV in the high range. The nominal operating range of the slow shaper and associated track/hold circuitry is from 0.100 V ("pedestal") to 2.5 Volts.

9.5 Discriminator Threshold Range

The GCFE contains 5 DACs to program discriminator thresholds. The characteristics of the range of programmability for each DAC is defined in Table 14. Note that the fast low energy discriminator DAC, FLE_DAC is a 7 bit DAC with two differ ranges determined by the most significant programming bit – the range select bit. Each DAC functionality is shown in MeV (assuming nominal light yields and gain) and in millivolts. Note that the DACs (except the RNG_ULD_DAC) have a 100 mV pedestal. The typical thresholds are shown in MeV and DAC level selection number.

Table 14. Discriminator DAC Programmability

Discriminator DAQ	Typical Threshold (MeV) (Sel #)	Full Range (MeV) (mV)	% of Full Range	Typical Noise (MeV) (mV)	Low Limit of Range (MeV) (mV)	High Limit of Range (MeV) (mV)	Resolution (MeV) (mV)	Range Select bit	Number of Bits
LOG_ACPT_DAC	2	200	26%	0.4	0	53	0.41	n/a	7
	5	2500		4.8	100	735	5.00		
FLE_DAC (test)	5	1600	3%	1.6	0	52.5	0.82	0	6
	6	2500		2.4	100	179	**1.25**		
FLE_DAC (nom)	100	1600	23%	1.6	64	367.5	4.74	1	6
	17	2500		2.4	100	651	**8.75**		
FHE_DAC	1000	100000	13%	80	0	13229	103.35	n/a	7
	10	2500		1.92	100	418	2.50		
RNG_ULD_DAC	2500 mV	-	32%	-	-	-	-		7
	87	2750			1980	2742	6.00		
REF_DAC	100 mV	-	106%	-	-	-	-	n/a	7
	0	2640			100	2640	20.00		

10 Addressing

The address of a GCFE chip on a layer is determined by the five input signals, RIGHT_FIRST and the four ADDR[3:0] bits. Table 15 defines the command address with respect to the state of these five input signals.

Table 15. Chip Address Decoding Definitions

RIGHT_FIRST	ADDR3	ADDR2	ADDR1	ADDR0	Address field in Command
0	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	none
	1	1	0	1	none
	1	1	1	0	none
	1	1	1	1	all
1	0	0	0	0	11
	0	0	0	1	10
	0	0	1	0	9
	0	0	1	1	8
	0	1	0	0	7
	0	1	0	1	6
	0	1	1	0	5
	0	1	1	1	4
	1	0	0	0	3
	1	0	0	1	2
	1	0	1	0	1
	1	0	1	1	0
	1	1	0	0	none
	1	1	0	1	none
	1	1	1	0	none
	1	1	1	1	all

11 Pin Names

Table 16. Input Pin Definitions

HE_SIG_IN:	High-Energy Diode Signal
HE_SIG_RET:	High-Energy Diode Return
LE_SIG_IN :	Low-Energy Diode Signal
LE_SIG_RET:	Low-Energy Diode Return
CALIB_STRBP :	Calstrobe plus. 2k ohm input protection on pad.
CALIB_STRBM :	CalStrobe minus. 2k ohm input protection on pad.
CALIB_V_SIG :	Calibration Voltage Signal
CALIB_V_ RET :	Calibration Voltage Return, nominally connected to AGND.
RESETP:	Reset plus. 2k ohm input protection on pad.
RESETM :	Reset minus. 2k ohm input protection on pad.
CMDP :	Command plus. 2k ohm input protection on pad.
CMDM :	Command minus. 2k ohm input protection on pad.
DAQ_CLKP:	DAQ_Clock plus. 2k ohm input protection on pad.
DAQ_CLKM:	DAQ_Clock minus. 2k ohm input protection on pad.
START_ACQP	Start Acquisition plus. 2k ohm input protection on pad.
START_ACQM:	Start Acquisition minus. 2k ohm input protection on pad.
RIGHT_FIRST:	right/left addressing indicator (see Table 15 for meaning)
ADDR3:	Address bit 3 to select chip on layer
ADDR2:	Address bit 2 to select chip on layer
ADDR1:	Address bit 1 to select chip on layer
ADDR0:	Address bit 0 to select chip on layer
ANA_RESET	Front end reset control. Internal automatic preamp reset circuit enabled by floating pin. Automatic preamp reset disabled by grounded pin.
REF_X8	Voltage reference for x8 T&H and baseline for other analog circuits. Pin may later be made AGND.

Table 17. Current-setting Pin Definitions

I_FET	Pin to adjust current for front-end FET. Nominal 15.0k ohms resistance to 3.3V.
I_BIAS	Analog circuits current mirror reference. Nominally external 500k ohms resistance to 3.3V.
BIAS_P	LVDS Driver input. Default LVDS driver current is 0.4 mA. Each external 7k ohm to ground adds 0.2 mA in LVDS driver current, up to a maximum of 1.2 mA. This pin may later be made to digital ground.

Table 19. Preamp/Shaper Pin Definitions

LE_PREAMP_OUT	LE preamp output
LE_SHPR_OUT	LE slow shaper output
HE_PREMP_OUT	HE preamp output
HE_SHPR_OUT	HE slow shaper output

Table 18. Power Pin Definitions

AVDD	Analog VDD, nominally 3.3 Volts
DVDD	Digital VDD, nominally 3.3 Volts
V_GUARD	Output voltage equal to preamp input voltage. Used to drive leakage protection guard rings around preamp inputs.
AGND	Analog ground
DGND0	Digital ground
DGND1	Digital ground

Table 20. Output Pin Definitions

DIG_DAT_OUTP :	Digital data output plus
DIG_DAT_OUTM :	Digital data output minus
ANALOG_OUT :	Analog signal output
LE_DISCP:	Low Energy Discriminator output plus
LE_DISCM:	Low Energy Discriminator output minus
HE_DISCP:	High Energy Discriminator output plus
HE_DISCM:	High Energy Discriminator output minus Shaper IO

12 Pin Numbers

Figure 9 shows the pin assignments for version 7 of the GCFE ASIC mounted in a 44 pin Quad Flat Pack.

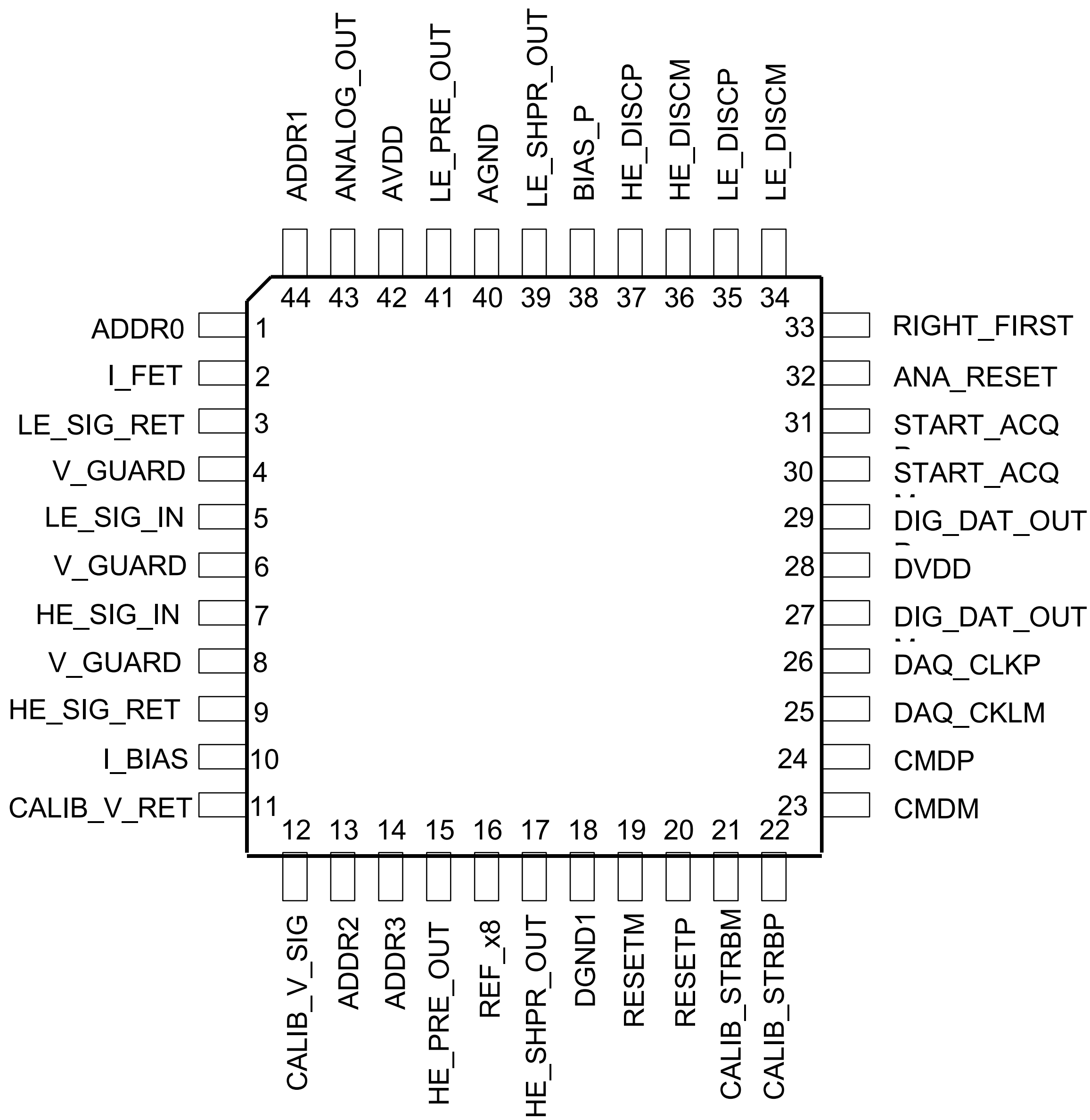

Figure 9. GCFE Ver 7 Pin Assignments - 44 Pin QFP