

REQUEST FOR ACTION (RFA) RESPONSE

**GLAST LAT Project
Calorimeter Peer Review**

17 – 18 March 2003

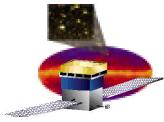
Action Item:	CAL – 014
Presentation Section:	Thermal
Submitted by:	Tom McCarthy

Request: Thermal qualification - Consider presenting thermal analysis using Qual Level boundary conditions. This applies to both box and board level analyses.

Reason / Comment: Thermal design goals is to ensure critical part temperatures stay below derated limits, that ensure the life of the parts in the qualification environment.

Response: 27 June 2003

The analyses and charts presented in response to RFA CAL-009 also provided the thermal analysis results at the qual level boundary conditions. These charts are attached here.



AFEE Thermal Analysis

- AFEE Thermal Analysis Summary. Dated 4/03 Author Peck Sohn, Swales Aerospace
- Table of maximum silicon die temperature for 25 C Base Plate temperature

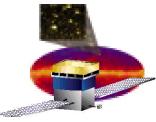
Device	GCRC	GCFE	ADC	DAC	Ref.
Die Junction Temp. Degrees C	36.7	33.5	33.8	33.8	35.1

- Analysis result, Calorimeter AFEE electronics do not have any thermal problems

Assumptions

28.3	30.1	28.0
29.5	32.4	29.0
29.7	33.3	29.1
28.9	31.8	28.4
26.8	29.1	26.6

	Modeled Heat Dissipation	Theta Junction to Board (C/W)
GCRC	65 mW	50
GCFE	11.5 mW	114
ADC	2 mW	183
DAC	4 mW	86
Ref.	7 mW	232
Total Power per AFEE	952 mW	
AFEE PCB, Qty 2 of 1.4 mil thick Copper Thermal Plane Layers.		
Naval Research Lab Washington DC		



AFEE Thermal Analysis

- AFEE Thermal Analysis Summary.** Dated 4/03 Author Peck Sohn, Swales Aerospace
- Table of maximum silicon die temperature for 50 C Base Plate tem perature**

Device	GCRC	GCFE	ADC	DAC	Ref.
Die Junction Temp. Degrees C	61.3	58.2	58.5	58.4	59.7

- Analysis result, Calorimeter AFEE electronics do not have any thermal problems**

