

LAT Calorimeter Subsystem Peer Design Review

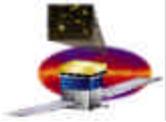
27 July 2001

Naval Research Laboratory
Washington DC



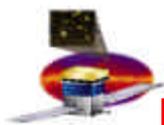
Review Agenda

9:00 AM	Introductions and Welcome	J. D. Kurfess	10
9:10 AM	Review Committee Introductions & Charge	Thurston	10
9:20 AM	Calorimeter Overview		80
	Design Overview	Johnson	10
	International Organization and Responsibilities	Johnson	10
	CAL-LAT Interfaces (and responsibilities)	Johnson	10
	Calorimeter Design (Csl, PIN, CDE, PEM, AFEE)	Phlips	30
	CAL Systems Requirements	Phlips	20
10:40 AM	Pre Electronics Module (PEM)		95
	Csl Crystals	Phlips	15
	Mechanical Design	Ferreira	30
	Thermal Design	Ferreira	10
	Crystal Detector Elements	Bédérède	20
	PEM Assembly and Test	Bogaert	20
12:15 PM	Lunch		60
1:15 PM	Electronics Design	Ampe	55
	Electronics Overview & Requirements		15
	Development Program		20
	Interfaces & Issues		20
2:10 PM	Assembly, Test and Calibration	Grove	50
	Module A&T		40
	Verification Matrix		10
3:00 PM	Safety and Mission Assurance	Virmani	45
3:45 PM	EM Development Plan	Johnson	15
4:00 PM	Committee Caucus		



Calorimeter Subsystem Overview

W. Neil Johnson
CAL Subsystem Manager
NRL



Large Area Telescope (LAT) Design Overview

Instrument

16 towers \Rightarrow modularity

height/width = 0.4 \Rightarrow large field-of-view

Tracker

Si-strip detectors: 228 μm pitch, total of 8.8×10^5 ch.

Calorimeter

hodoscopic CsI crystal array

\Rightarrow cosmic-ray rejection

\Rightarrow shower leakage correction

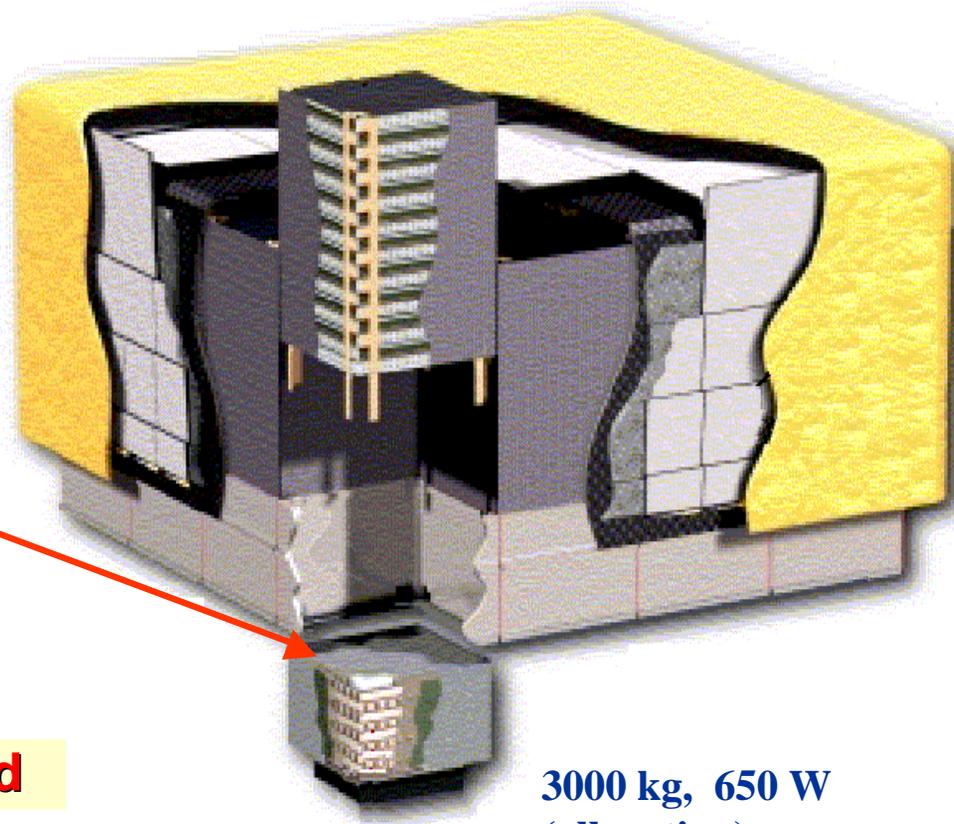
$X_{\text{Tkr} + \text{Cal}} = 10 X_0 \Rightarrow$ shower max
contained < 100 GeV

Anticoincidence Detector Shield

segmented plastic scintillator

\Rightarrow minimize self-veto

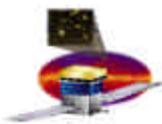
> 0.9997 efficiency & redundant readout



3000 kg, 650 W
(allocation)

1.75 m \times 1.75 m \times 1.0 m

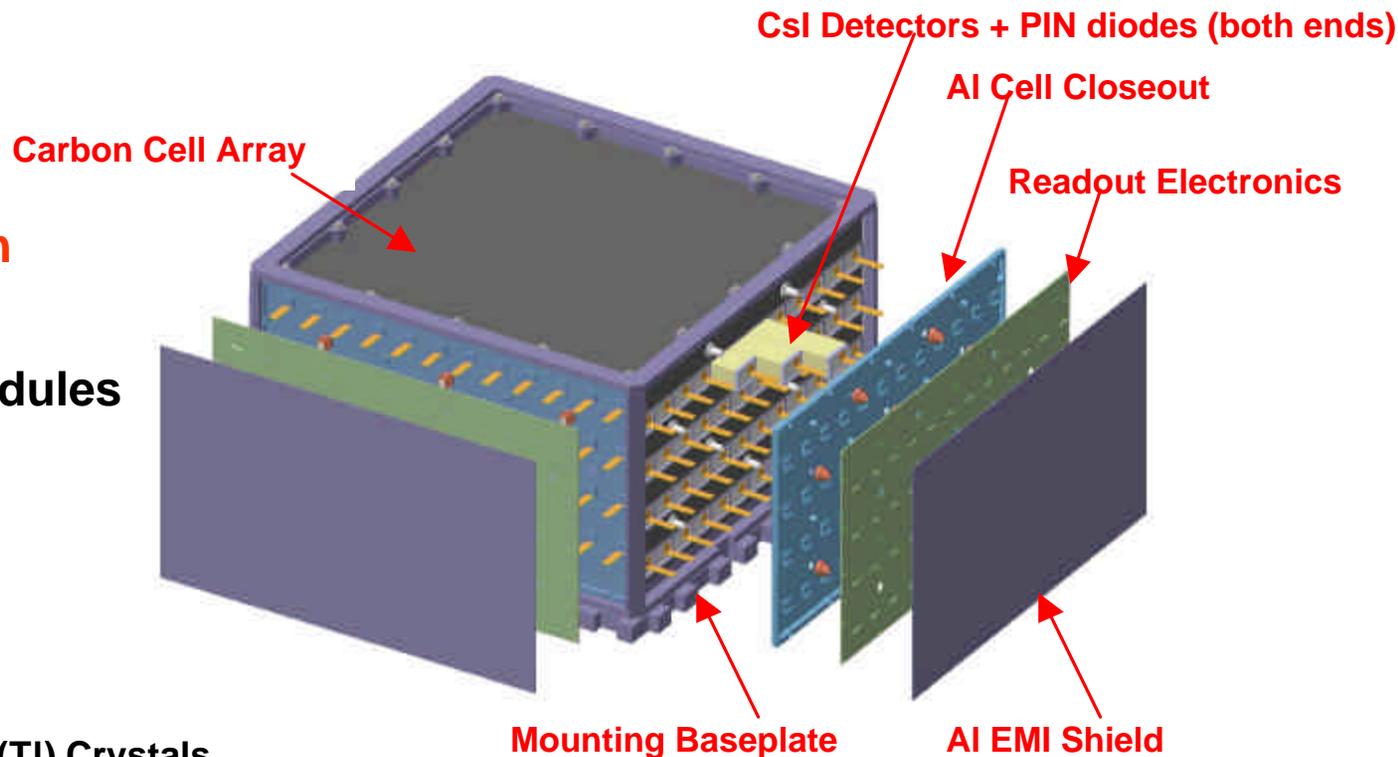
20 MeV – 300 GeV



Calorimeter Module Overview

Modular Design

4 x 4 array of
calorimeter modules



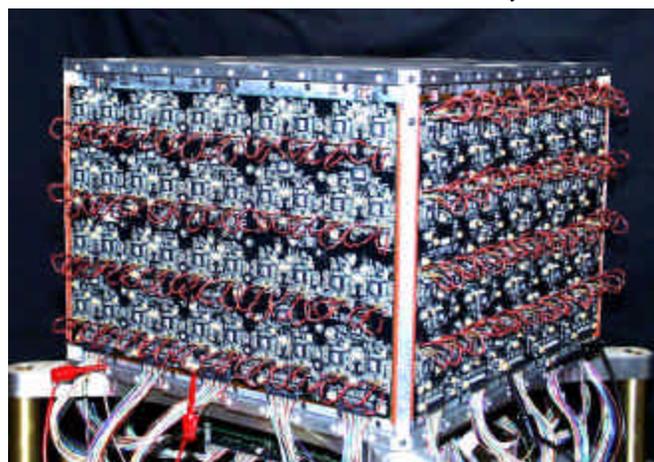
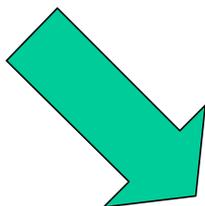
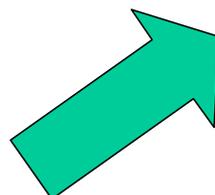
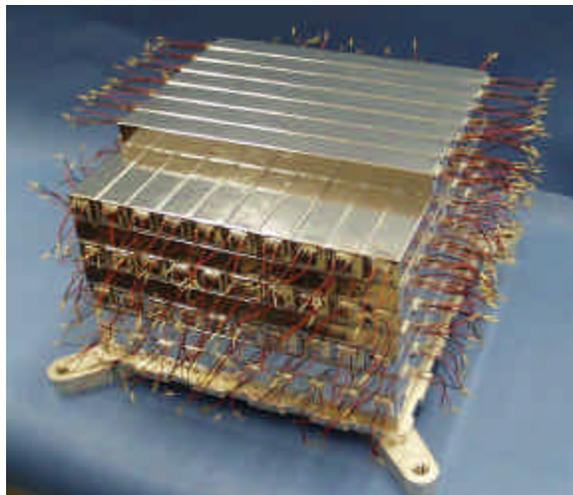
Each Module

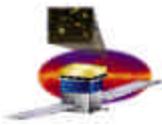
- ❑ 8 layers of 12 CsI(Tl) Crystals
 - Crystal dimensions: 27 x 20 x 333 mm
 - Hodoscopic stacking - alternating orthogonal layers
- ❑ Dual PIN photodiode on each end of crystals.
- ❑ Mechanical packaging – Carbon Composite cell structure

- ❑ Electronics boards attached to each side.
- ❑ Electronic readout to connectors at base of calorimeter.
- ❑ Outer wall is EMI shield and provides structural stiffness as well.



Beam-Test Prototype Calorimeter Assembly





Calorimeter Technical Challenges

- ❑ **Imaging calorimetry to support background rejection and to improve energy measurement via shower profile correction or leakage estimation.**
 - Hodoscopic arrangement of CsI crystals, 8 layers of 12 crystals
 - Longitudinal positioning in individual crystals using light asymmetry measurements at each end of crystal

- ❑ **Large dynamic range ($\sim 5 \times 10^5$) with low power electronics**
 - Divide signal into two ranges using dual PIN Photodiode of differing areas
 - Custom CMOS ASIC front end electronics

- ❑ **Minimize passive material and gaps in active material caused by modular design, yet survive 6g launch loads.**
 - Carbon composite structure with individual cells for each CsI crystal.
 - PIN diode readout via PCB on four sides of module.
 - EMI/structural outer wall.

- ❑ **Low dead time (< 20 msec), low power spectral measurements over full energy range.**
 - Dedicated ADC for each CsI crystal end
 - COTS low-power successive approximation ADCs

- ❑ **In-flight calibration**
 - Use cosmic rays (p – Fe)



CAL Level III Requirements

Parameter	Requirement	Verification	Expected Performance
Energy Range	5 MeV – 300 GeV 1 MeV – 1 TeV (goal)	Simulation	~2 MeV, beginning of mission (TBR)
Energy Resolution (1 sigma)	< 20% (20 MeV < E < 100 MeV) < 10% (100 MeV < E < 10 GeV) < 6% (10 GeV < E < 300 GeV, incidence angle > 60 deg)	Simulations and EM and LAT calib unit Beam Tests	TBD - smulations
Energy Resolution (1 sig) Single Crystal	< 1% for Carbon Ions of energy >100 MeV/nuc at a point.	EM (and Calib Unit) beam test	< 0.5% (correlation of ends removes Landau)
Design	Modular, hodoscopic, Csl > 8.4 RL of Csl on axis	Inspection	> 8.5 RL
Active Area	>1050 cm ² per module < 16% of total mass is passive mtrl.	Inspection	>1100 cm ² per module
Position Resolution	<1.5 cm in 3 dims, min ionizing particles, incident angle < 45 deg.	Test with cosmic muons, all modules	< 1.75 cm in longitudinal measurement
Angular Resolution	7.5 $\sqrt{\cos(q)}$ deg, for cosmic muons in 8 layers	Test with cosmic muons, all modules	8.5 $\sqrt{\cos(q)}$ deg
Dead Time	< 100 ms per event < 20 ms per event (goal)	Test	< 19 ms per event
Low Energy Trigger	>90% efficiency for 1 GeV photons traversing 6 RL of Csl < 2 ms trigger latency	Simulations	> 93% < 1 ms
High Energy Trigger	>90% efficiency for 20 GeV photons depositing at least 10 GeV < 2 ms trigger latency	Simulations, Calib unit test in beams	> 91% < 1 ms



CAL Level III Requirements (cont)

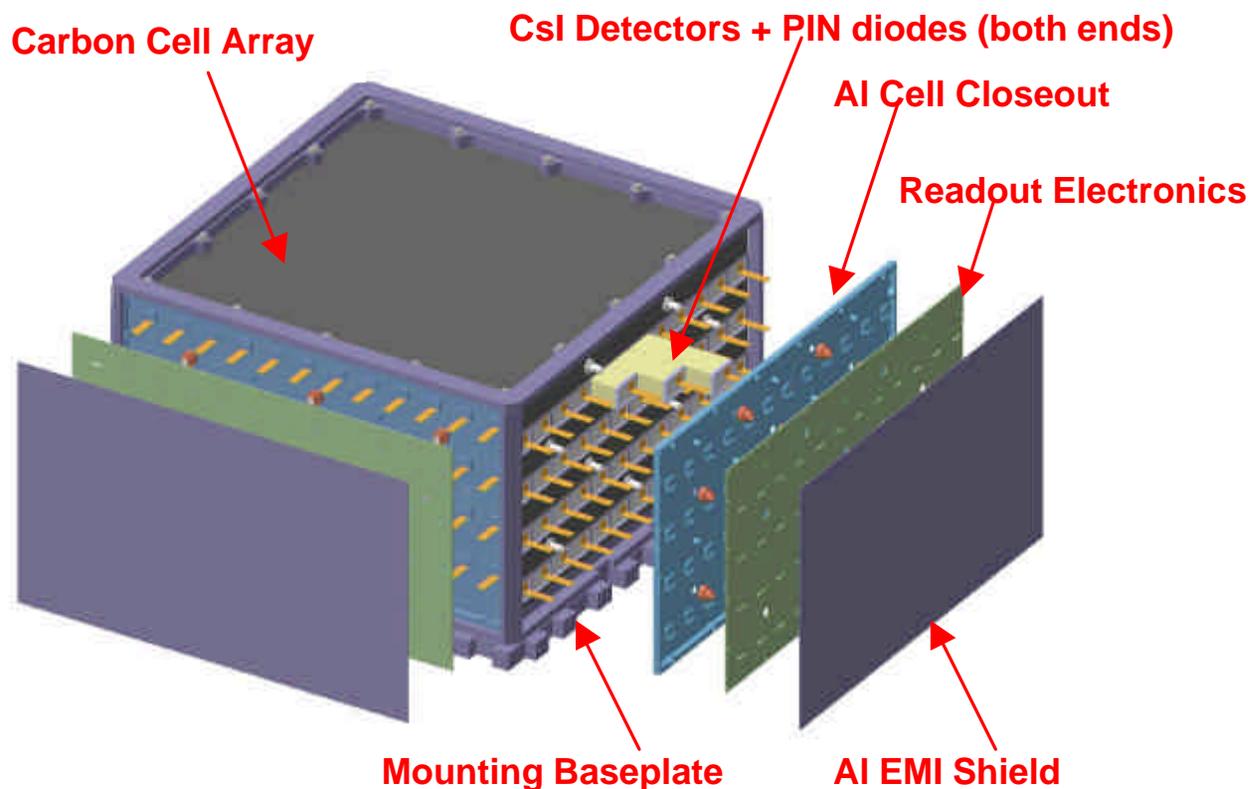
Parameter	Requirement	Verification	Expected Performance
Size (module)	< 364 mm in width (stay clear) < 224.3 mm in height (stay clear)	Inspection	363 mm 224 mm
Mass	< 1492 kg (93.25 kg/module)	Test	< 1476 kg
Power	< 91 Watts (conditioned) (5.69 W/module)	Test	< 62 Watts
Launch Environment	GEVS Requirements ± 3.5 g / ± 6 g, thrust static ± 4 / ± 0.1 g, lateral static	Primary structure, Test	Required performance
Temperature Range	- 10 to +25 C, operational - 20 to +40 C, storage - 30 to +50 C, operational	Subsystem TV Test, 4 cycles	Required performance
Instrument Lifetime	>5 yrs, with no more than 20% degradation.	Analysis	Required performance

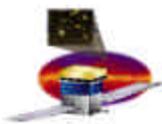


Calorimeter Module Overview

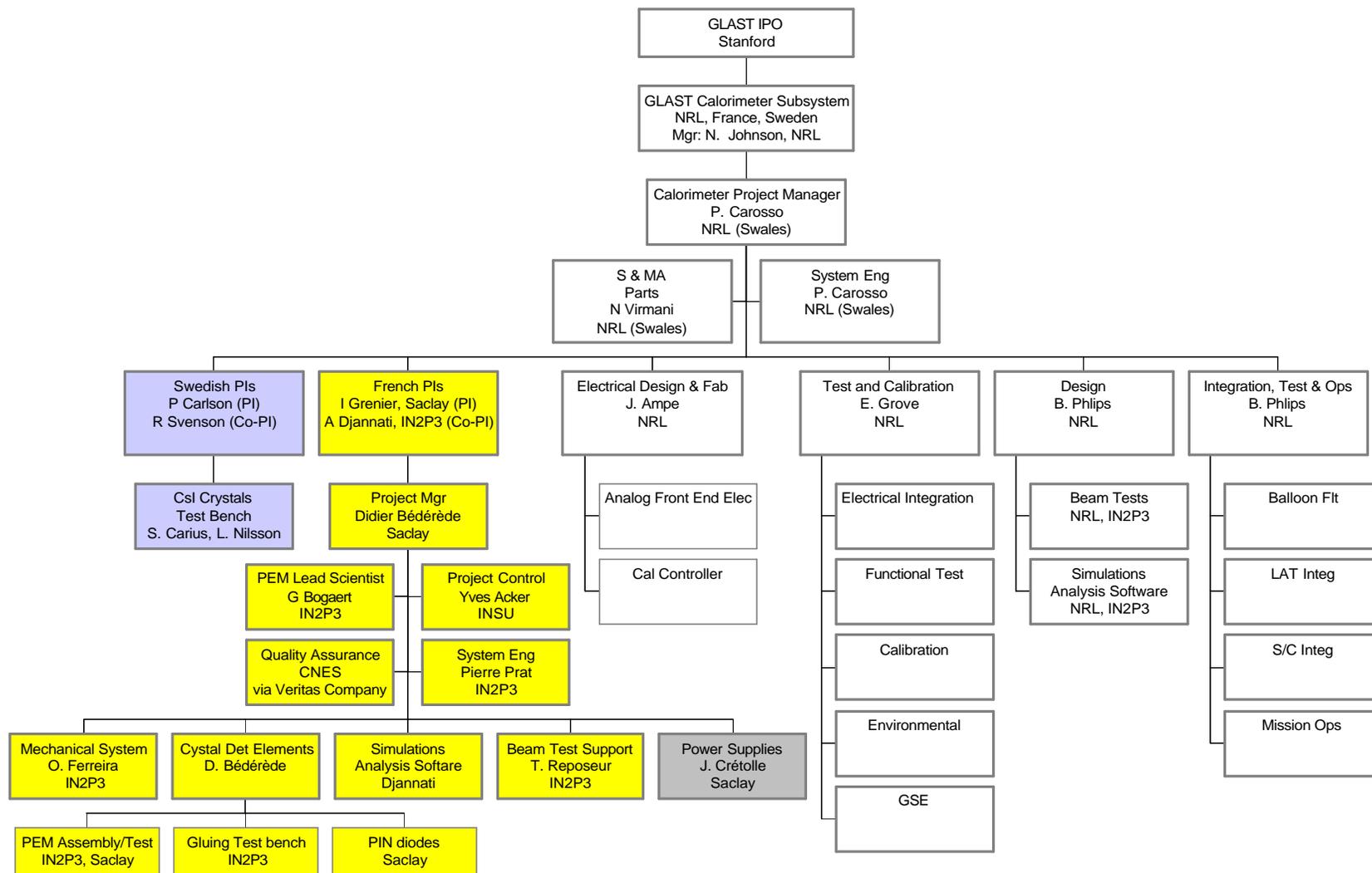
Responsibilities

- ❑ NRL provides CAL Program Lead and Mgmt
- ❑ Sweden buys and tests the CsI crystals
- ❑ France buys and bonds PIN diodes to the crystals.
- ❑ France builds the mechanical structure
- ❑ France installs the crystal detectors into the structure.
- ❑ NRL builds and mounts the electronics
- ❑ NRL calibrates and integrates the finished calorimeter modules with French support



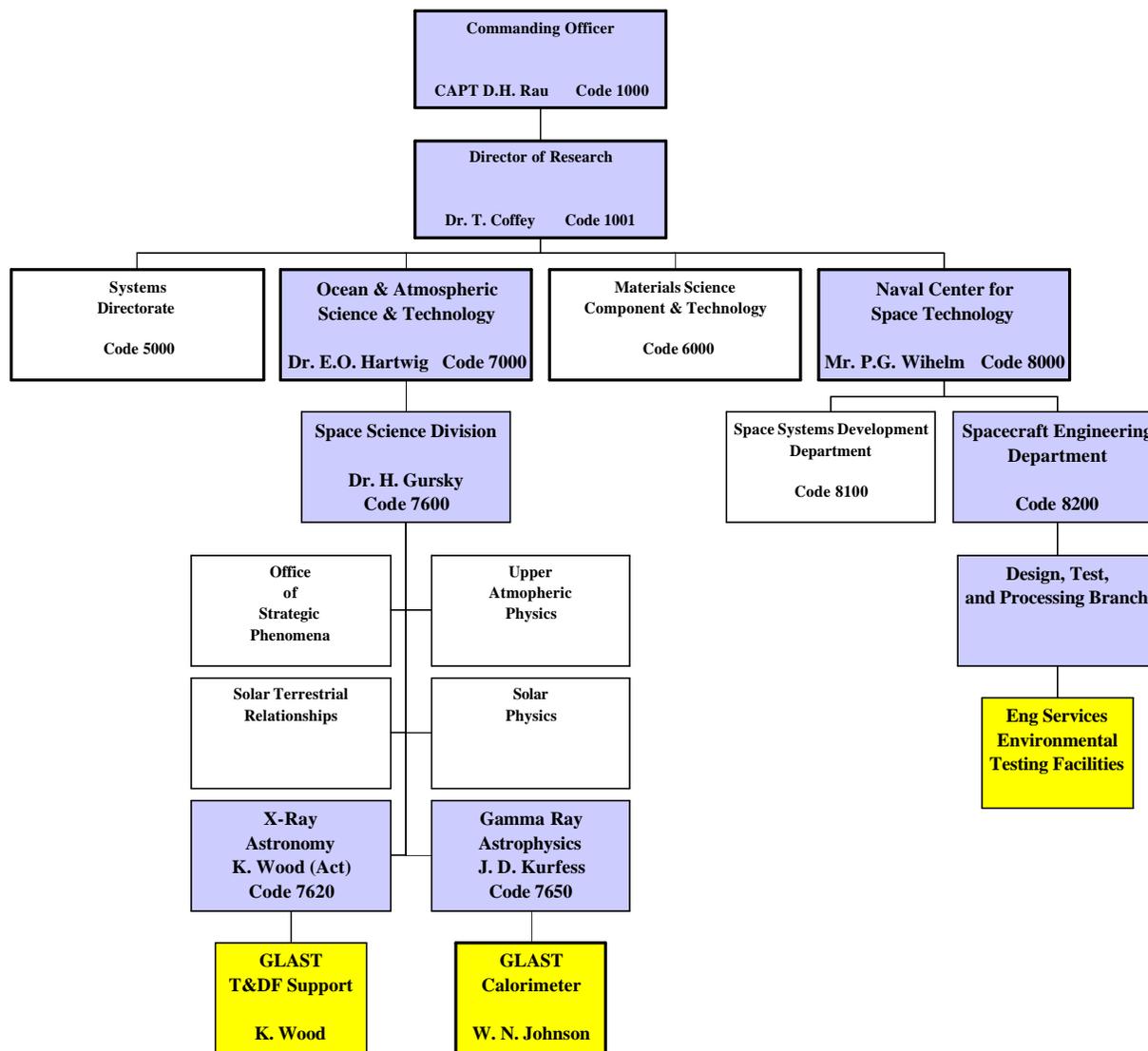


Calorimeter – Institutional Organization





Naval Research Lab Organization



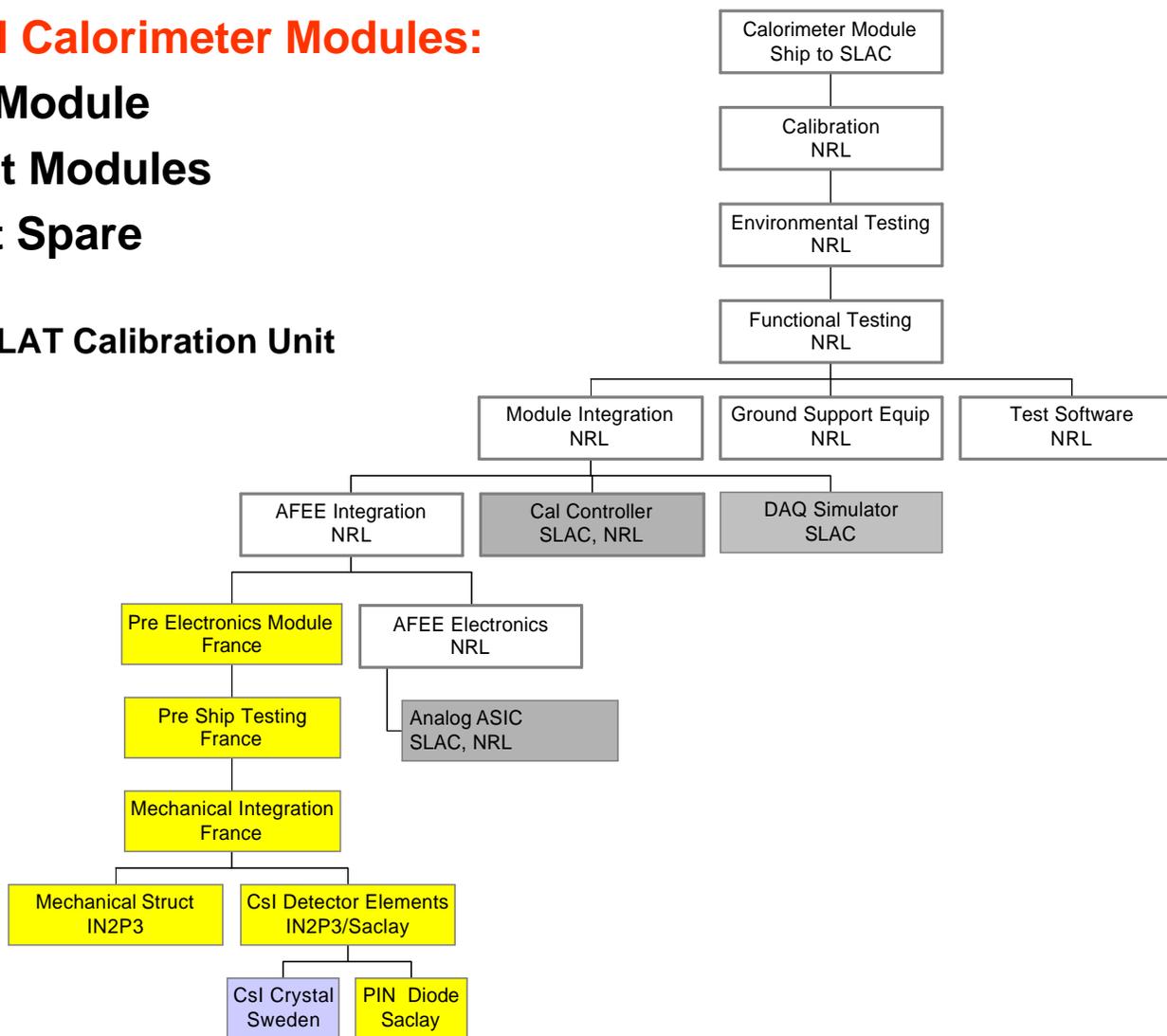


Calorimeter Module Assembly

18 Identical Calorimeter Modules:

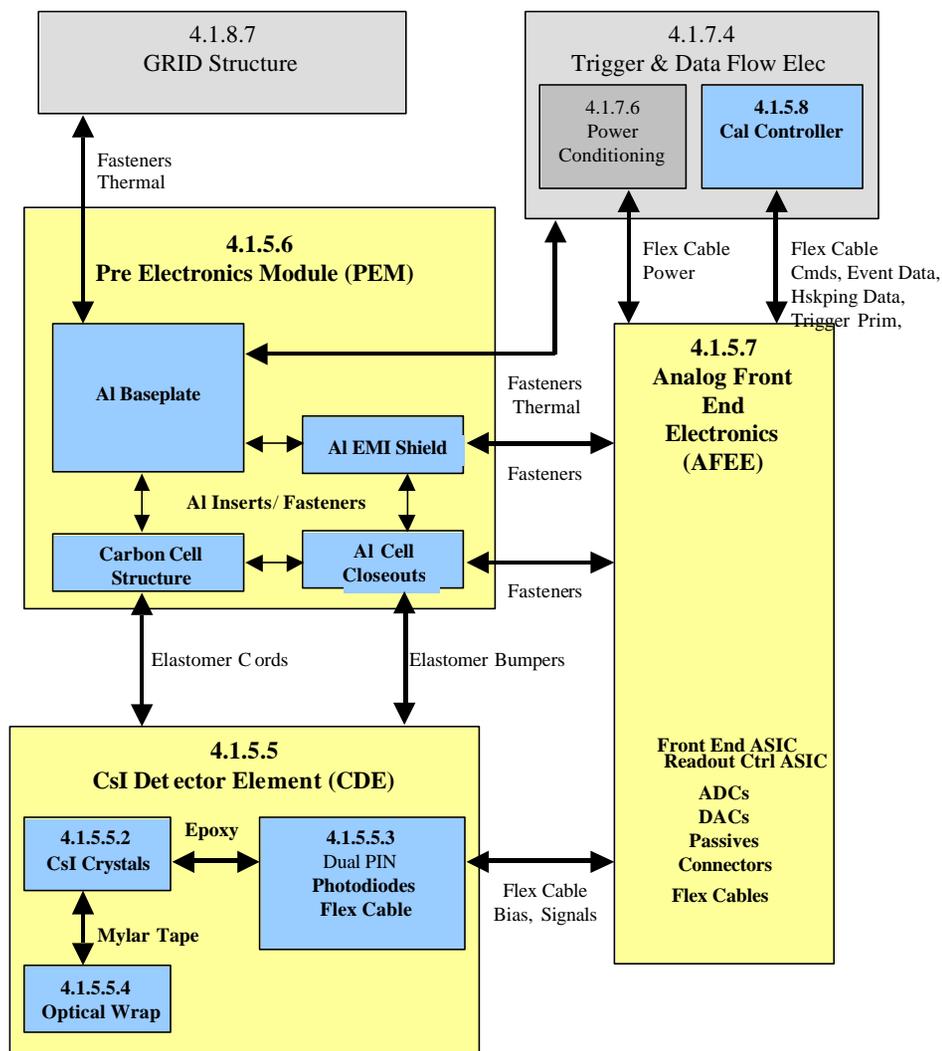
- 1 Qual Module
- 16 Flight Modules
- 1 Flight Spare

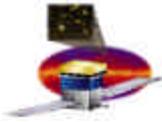
1st 4 units are LAT Calibration Unit





CAL Subsystem & External Interfaces





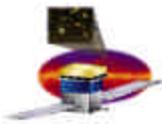
Calorimeter Design

Bernard Philips
Naval Research Laboratory



Concept

- ❑ **Silicon tracker is intrinsically very modular**
 - Calorimeter must support tracker readout geometry
 - The calorimeter needs to be modular as well (Fiberglass opposite)
- ❑ **Sampling, or non-sampling**
 - Low E performance rules out sampling
- ❑ **Imaging calorimeter desired for:**
 - Profile fitting
 - Calorimeter only events
 - Background rejection
- ❑ **Segmentation:**
 - Moliere radius is 38 mm
 - Radiation length is 18.5 mm
 - Need positioning on same order
 - Work out best segmentation:
 - Started out with longitudinal segmentation
 - Used one diode at each end
 - Found better position resolution along length
 - Changed to hodoscopic configuration



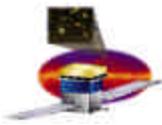
Concept Implementation

Detectors

- ❑ **Highly Segmented :**
 - No individual packaging, no NaI
 - CsI(Tl) next highest light yield available in bulk (LSO, YAP)
 - CsI(Tl) also best match for PIN diodes
- ❑ **PIN diodes: small, lightweight, low power, rugged**
- ❑ **Need careful packaging:**
 - Minimal passive material
 - Minimal gaps
 - Thermal expansion issues
 - Maximal light yield

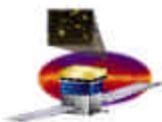
Electronics

- ❑ **Spectroscopy from MeVs to 100s of GeVs is demanding on electronics**
- ❑ **Large number of channels implies low power per channel by spectroscopy standards (number of channels x number of bits is 5×10^7)**
- ❑ **Need to minimize space for electronics**
- ❑ **Need to communicate to a common DAQ**

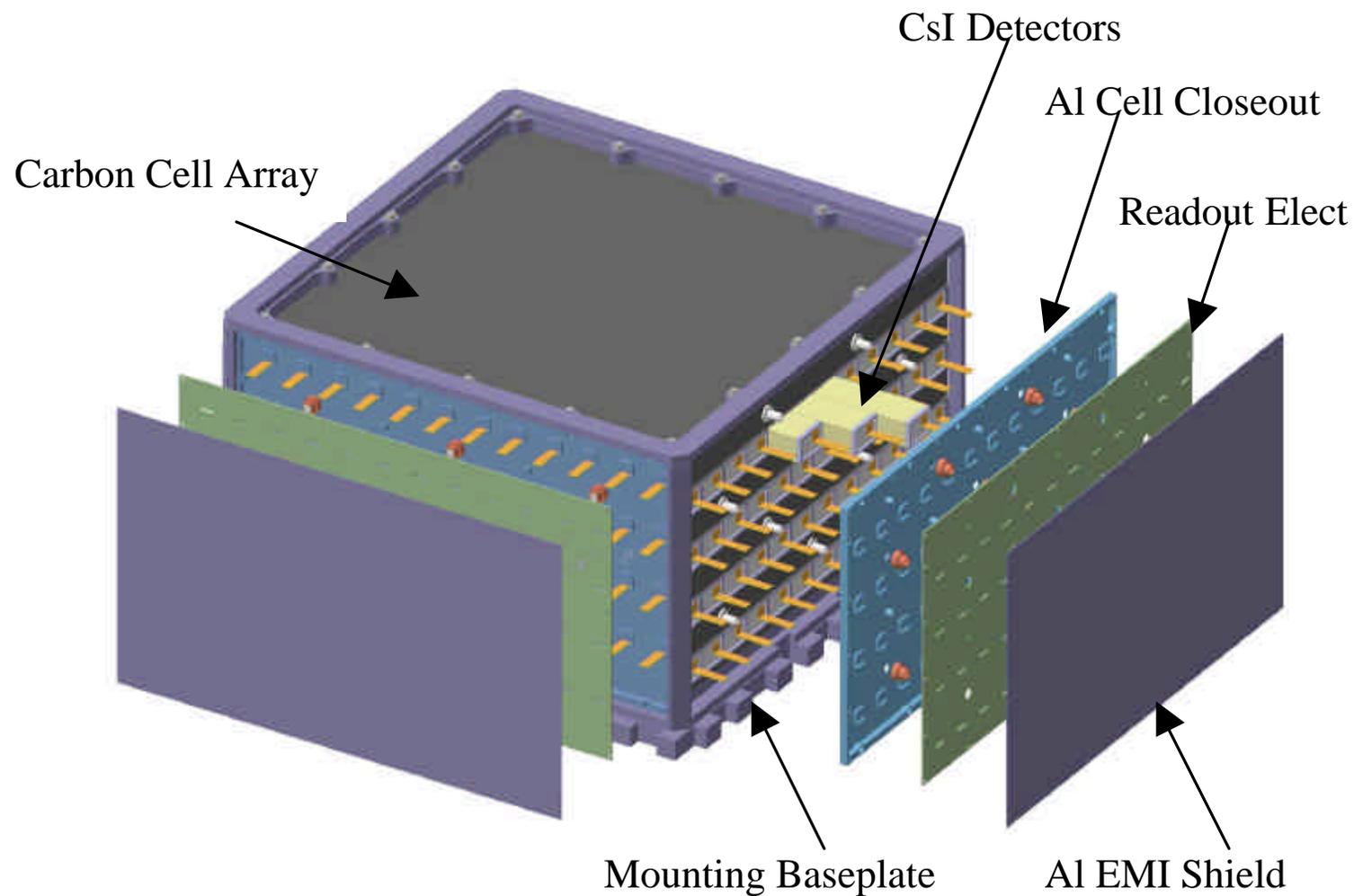


Design Specifics

- ❑ 16 towers, each with one calorimeter module
- ❑ 8.5 radiation lengths deep (8 layers)
- ❑ 96 crystals per calorimeter module (12 crystals across)
- ❑ Calorimeter module frontal area 363 mm x 363 mm
- ❑ Active frontal area 333 mm x 333 mm (1.5 cm passive rim)
- ❑ Height is 224 mm, 159 mm active (thick base plate for grid stiffness)
- ❑ 1 lightweight structure, holds ~ 80 kgs against 6gs with ~ 10 kgs
- ❑ Diodes at each end of CsI crystals (with tapered light yield)
- ❑ Design dual diodes because of dynamic range
- ❑ Design custom Analog and digital ASICs
- ❑ Four independent front end electronics boards
- ❑ Tower Electronics Module (TEM) common to tracker for digital readout to data acquisition system

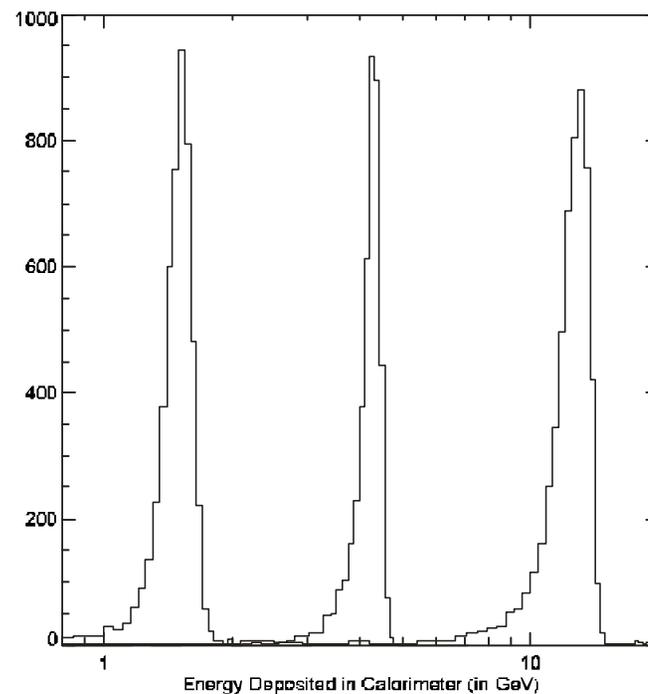
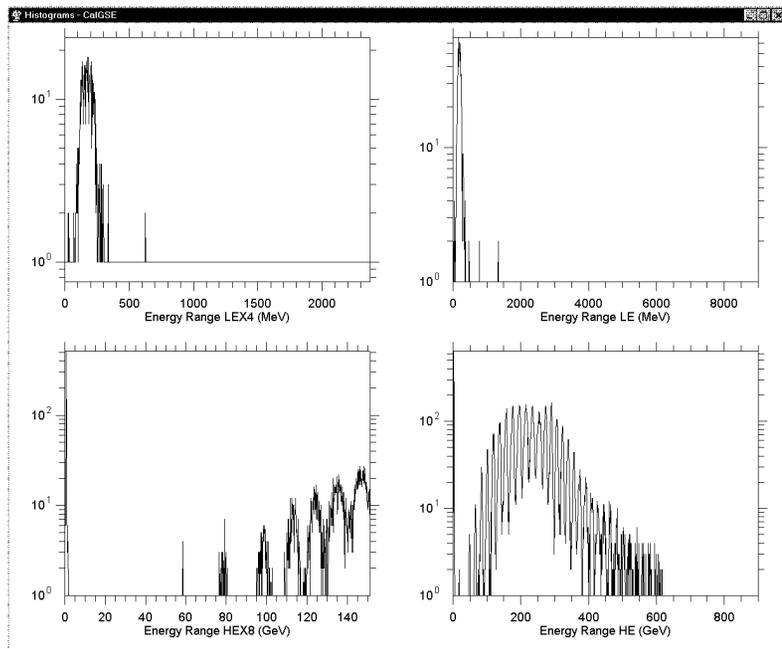


Exploded View





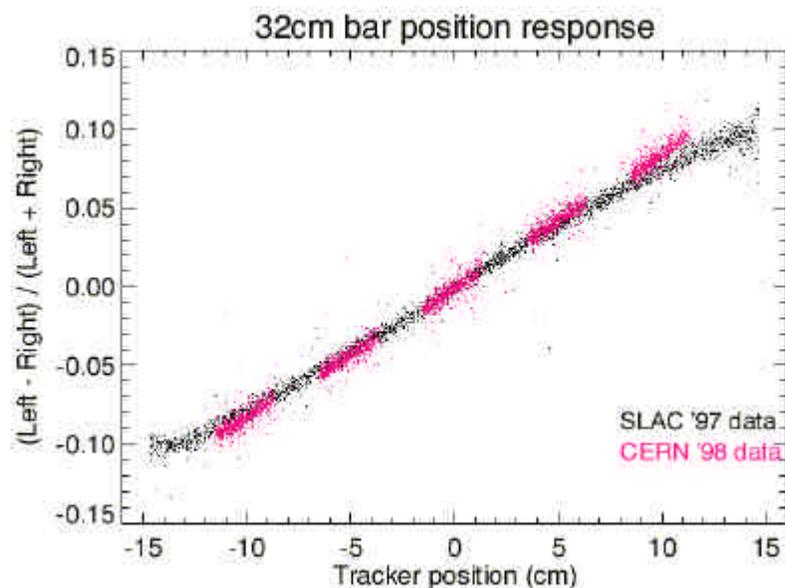
Calorimetry - Beam Test '99



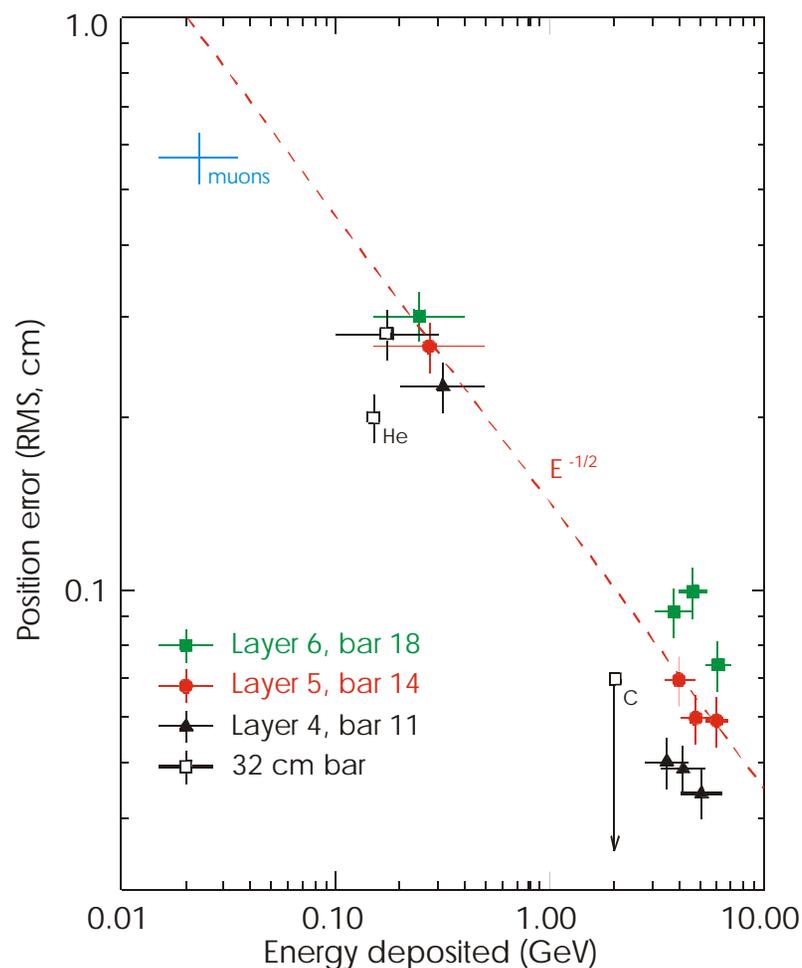
- ❑ Demonstrated from ~ 10 MeV in crystal to 600 GeV in calorimeter module
- ❑ Dominated by electronics at low energies
- ❑ Dominated by shower leakage at high energies
- ❑ Corrections from shower profile at high energies
- ❑ 7% resolution at 20 GeV



Calorimeter Positioning



- ❑ Use relative signal at each end of crystal to derive position $(L-R) / (L+R)$
- ❑ Can intrinsically achieve submillimeter positioning
- ❑ Scales as $E^{-1/2}$
- ❑ Limited by electronic noise or ADC quantization
- ❑ Worse after shower maximum
- ❑ Very good for cosmic rays

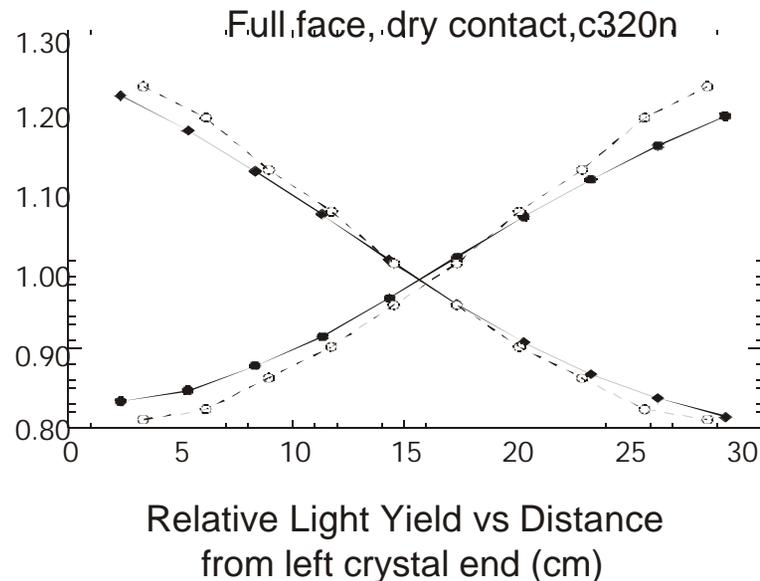




CsI(Tl) Crystals

Swedish Contribution

- Active material in Calorimeter
- 2040 crystals (1536 for flight)
- 333 mm x 19.9 mm x 26.7 mm
- ~ 1600 Kg of CsI
- CsI to provide high light yield
- Apply taper to light yield for longitudinal positioning
- Precise machining required
- Careful handling to preserve shape
- Beveled edges
- Need to characterize each crystal
 - Mechanically
 - Optically
- Radiation tests on each boule

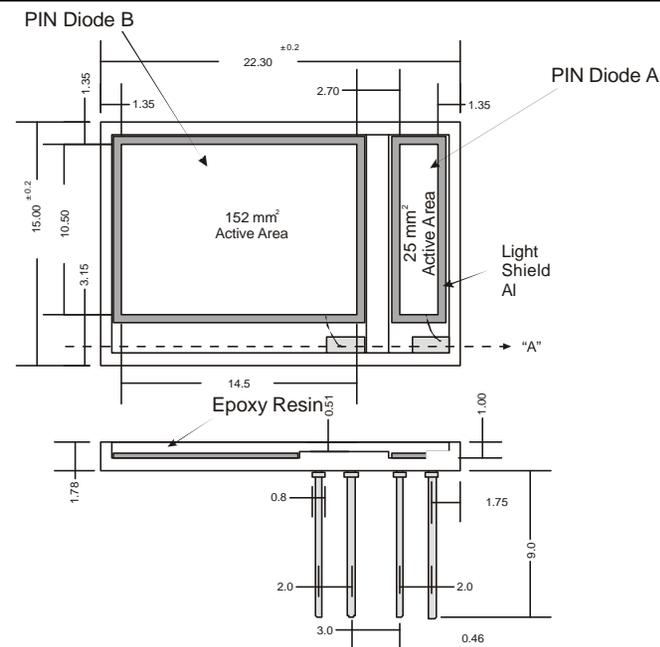




PIN diodes

French Contribution

- ❑ Very small mass
- ❑ Very small volume
- ❑ Very low power
- ❑ Rugged
- ❑ Made commercially in large quantities
- ❑ Customize dimensions for GLAST
 - Still standard manufacturing
- ❑ Implement two diodes on single carrier
 - Need multiple signals for AFEE
 - Single carrier for convenience
 - Need large diode for low energy work
 - Want small diode large enough for muons
 - Need flexible interconnect to AFEE



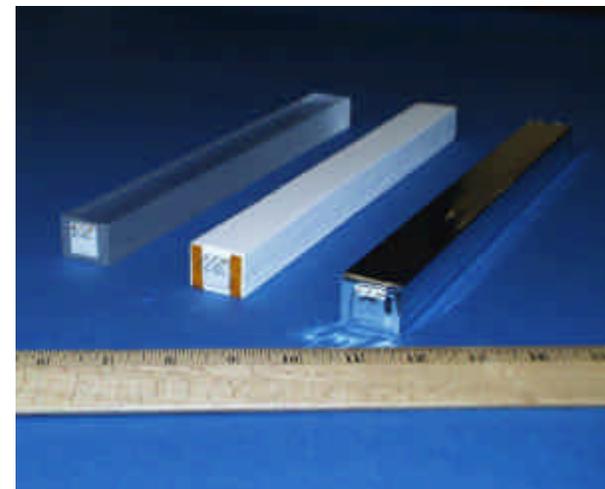
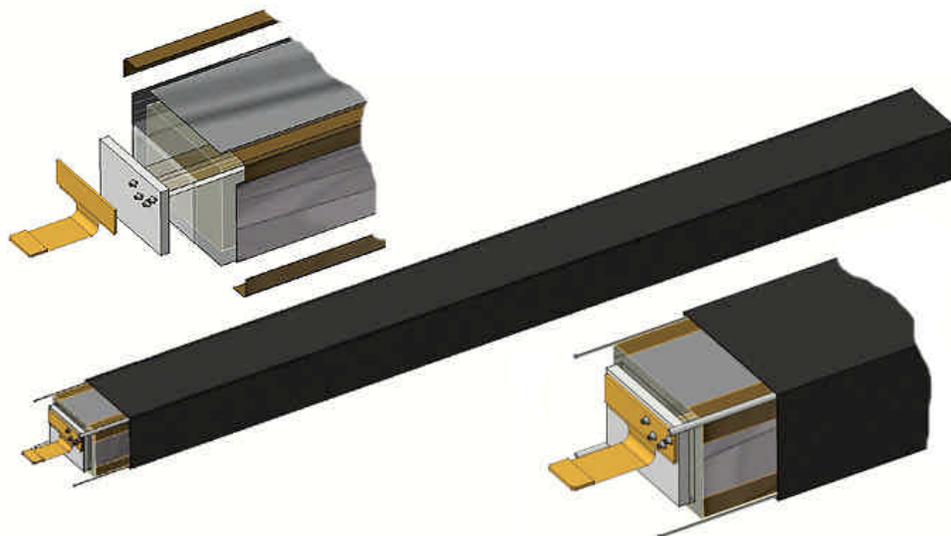
BTEM '99 Dual PIN Diodes
Hamamatsu Photonics
96 mm² and 24 mm²





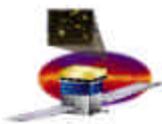
Crystal-Detector Element

French Contribution



BTEM '99 CDE

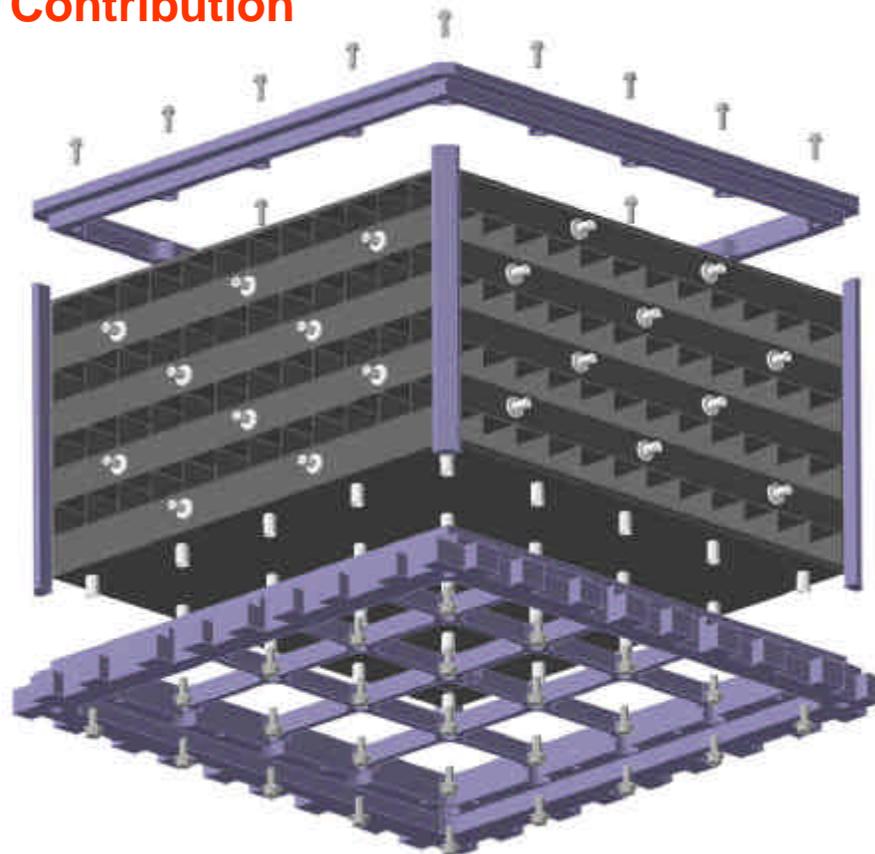
- ❑ **Crystal-PIN diode-Wrapper combination is called **Crystal Detector Element (CDE)****
- ❑ **Careful choice of wrapper to optimize light yield**
- ❑ **Careful choice of bonding material for PIN diode-crystal bond**
 - **Nature of crystal (performs like oil-coated lead) make adhesion difficult**
 - **CTE of crystal means preserving quality of bond through thermal cycling difficult**



Mechanical Structure

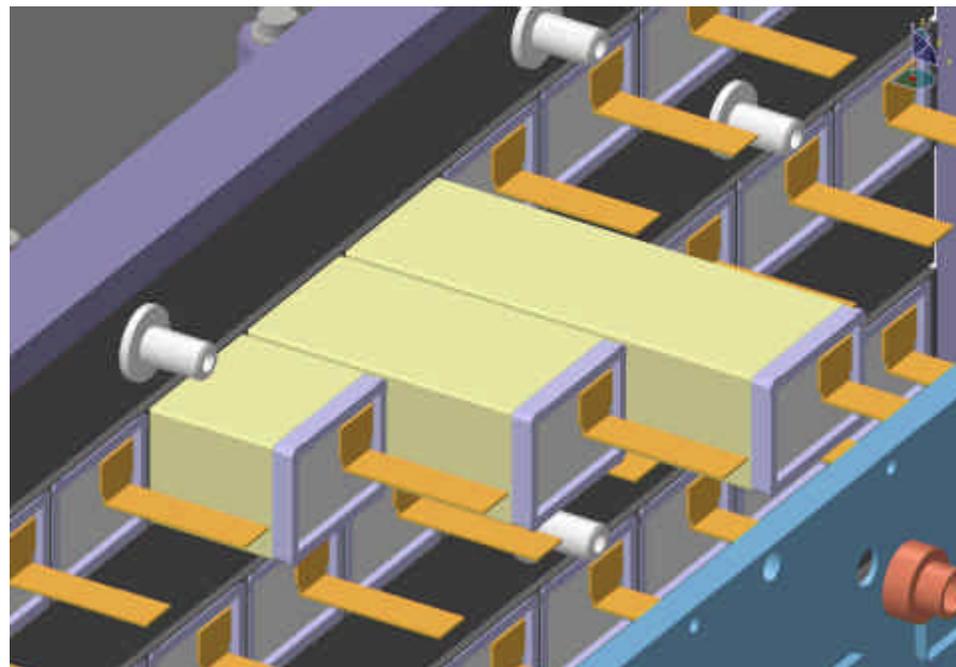
French Contribution

- Carbon fiber structure
- Must hold ~80 kg @ 6 g with ~ 10 kg
- Must be able to handle thermal expansion of CsI
- 96 individual cells
- Al top, bottom and side plate
- Bottom plate is stiffener for grid
- Bottom plate is mechanical support for TEMs and power supplies
- Sides support for AFEE

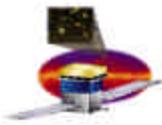




Pre-Electronics Module (PEM)



- ❑ Mechanical structure + CDE (Crystal Detector Element) is called PEM
- ❑ Crystal held in place by elastomeric cords and pads:
 - 4 cords at beveled edges of crystals
 - Pads at each end around PIN diodes
- ❑ Close-out plate pushes against all elastomeric pads
- ❑ Close-out plate also supports electronics boards



Electronics Design

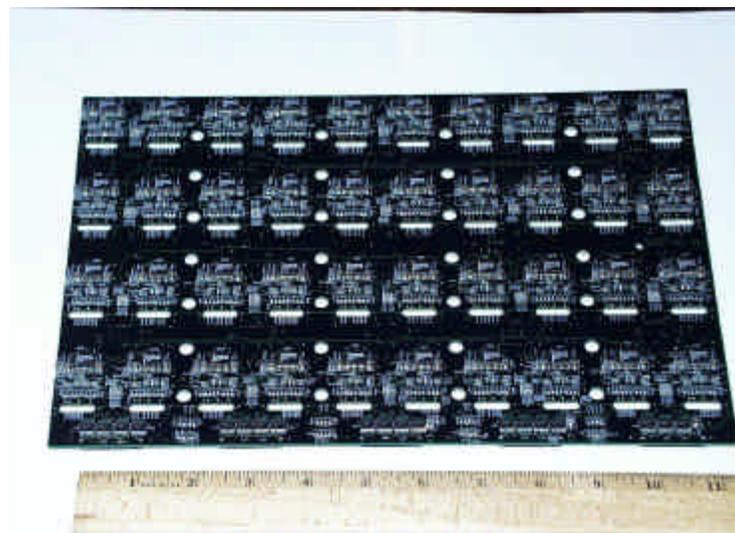
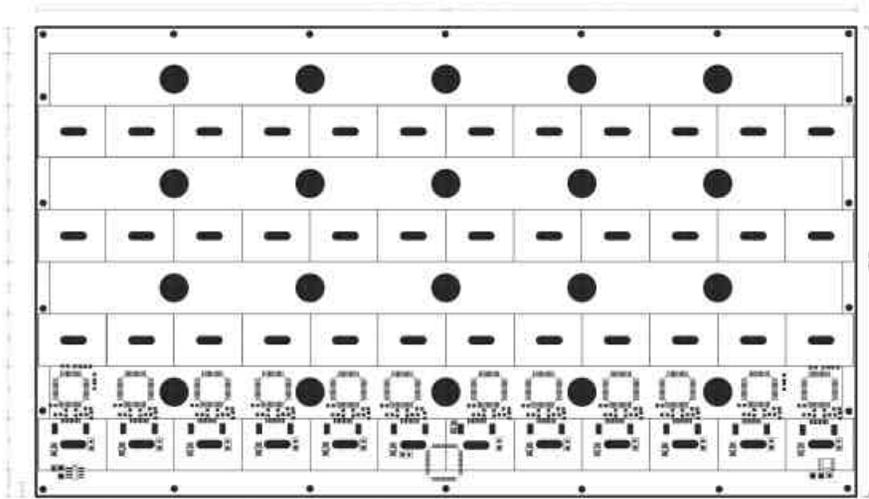
- Need to cover a very large dynamic range
 - Thresholds <1 MeV to 100s of GeV in calorimeter
- Low noise (2000 electrons noise)
- Low power (~ 20 mW per crystal end)
- Limited space (8 mm thickness), match pitch of CsI crystals (28x40 mm)
- Interface to TEM

- Use 1 custom analog and 1 custom digital ASIC to minimize power
- Use 2 input signals to reduce dynamic range requirement on electronics
 - Each input signal goes into 2 gain ranges
 - Have ranges to 200 MeV, 1.6 GeV, 12.5 GeV and 100 GeV
- Use commercial 12 bit ADCs (0.05, 0.4, 3, 24 MeV bins)
- Low dead time (20 ms)
- Sparsify data (zero suppress)



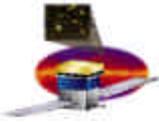
AFEE board design

NRL Contribution

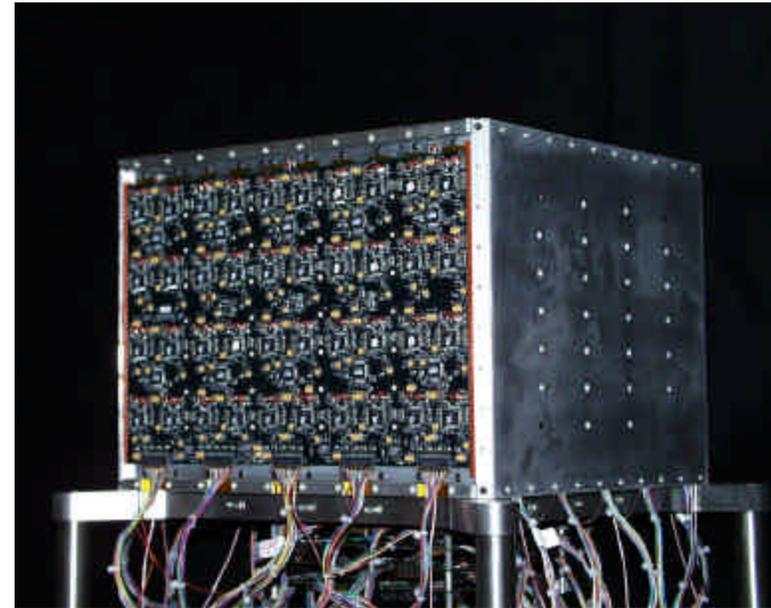
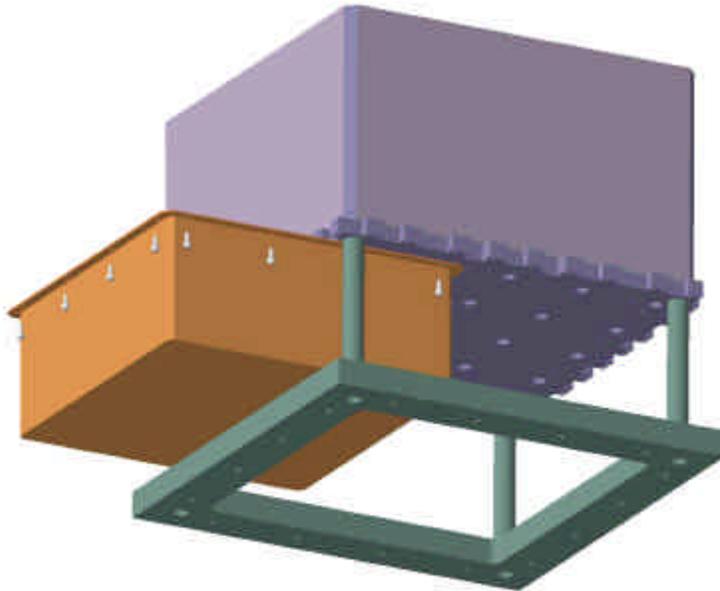


BTEM '99 AFEE Board

- ❑ 2 types of boards (X and Y)
- ❑ Connect to 48 crystal ends (96 PIN diodes)
- ❑ Provides -70V bias for diodes (from power supply)
- ❑ Hold 48 analog front end ASICs and 48 ADCs
- ❑ Hold 4 digital readout ASICs
- ❑ Hold external DAC for calibration and temperature sensor
- ❑ Components on both sides of board (only 3 mm for components)
- ❑ BTEM1999 boards had 1400 components
- ❑ BTEM1999 used GCFE designed by Goddard. Used peak detect



Calorimeter Module-TEM Integration



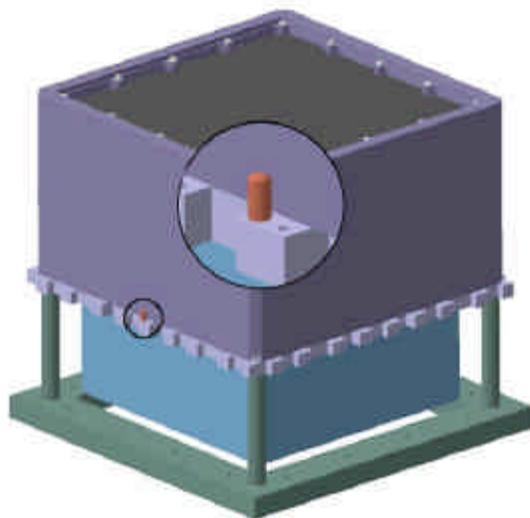
BTEM '99 Module

- TEM cards responsibility of SLAC (not part of calorimeter sub-system)
- Mount on Calorimeter Module baseplate
- Flex cables (not shown) will connect AFEE boards to TEM board
- Central tabs for calorimeter cables
- One box (TEM + Power Supplies) drawn here (TBD)
- Green fixture removed for flight

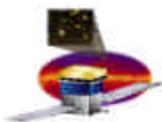


BTEM 1999-Fully Assembled

- ❑ Outer side plate provide EMI protection
- ❑ Flight digital electronics box will not covers tabs
- ❑ Align into grid with alignment pins



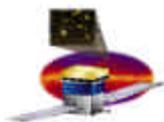
**BTEM '99 Completed Module
with shipping stand**



Mass Budget

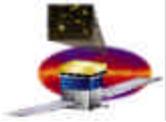
Component	Material	Mass (Kg)
Composite structure	Graphite epoxy	3.363
Structure shell	Aluminum	7.090
Dampers	Silicone	0.320
Fasteners		0.500
CDE	Csl, PIN diodes, flex cables	79.123
AFEE	Circuit card, ASICs	1.690
Miscalleneous		0.1
Total Mass of Cal		92.195
Calorimeter Allocation		93.250

Passive Material is 15% of total mass



Power Budget

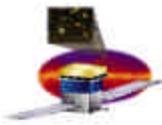
Item	Quantity	Power (mW)	
		Each	Total
GCFE	48	8	384
ADC Max145 (no sleep)	48	4	192
Digital Controller ASIC	4	80	320
DAC	1	6	6
DAC Buffers	4	5	20
References	2	5	10
LV Biasing	48	1	24
PIN Bias	1	1	1
TOTAL Power per AFEE (mW)			957
TOTAL Power per Module (mW)			3,828
Allocated Power per Module (mW)			5,688



Calorimeter Design

LEVEL III Requirements Compliance

Bernard Philips
Naval Research Laboratory



Level III - Geometry

- ❑ **Design:** Modular, hodoscopic,
Csl > 8.4 RL of Csl on axis

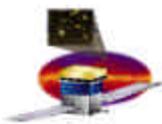
➔ Modular, 8.5 RL on axis

- ❑ **Active Area:** >1050 cm² per module
< 16% of total mass is passive material

➔ 1109 cm², 15% of total mass is passive material

- ❑ **Size (module):** < 364 mm in width (stay clear)
< 224.3 mm in height (stay clear)

➔ 363 mm x 363 mm, 224 mm height



Level III – Low Energy Trigger

□ Low Energy Trigger:

- >90% efficiency for 1 GeV photons traversing 6 RL of CsI
- < 2 ms trigger latency

→ 93% efficiency

- trigger consisting of an OR of logs in a tower
- 100 MeV threshold
- (from simulation)

→ < 1 ms trigger latency expected from GCFE design



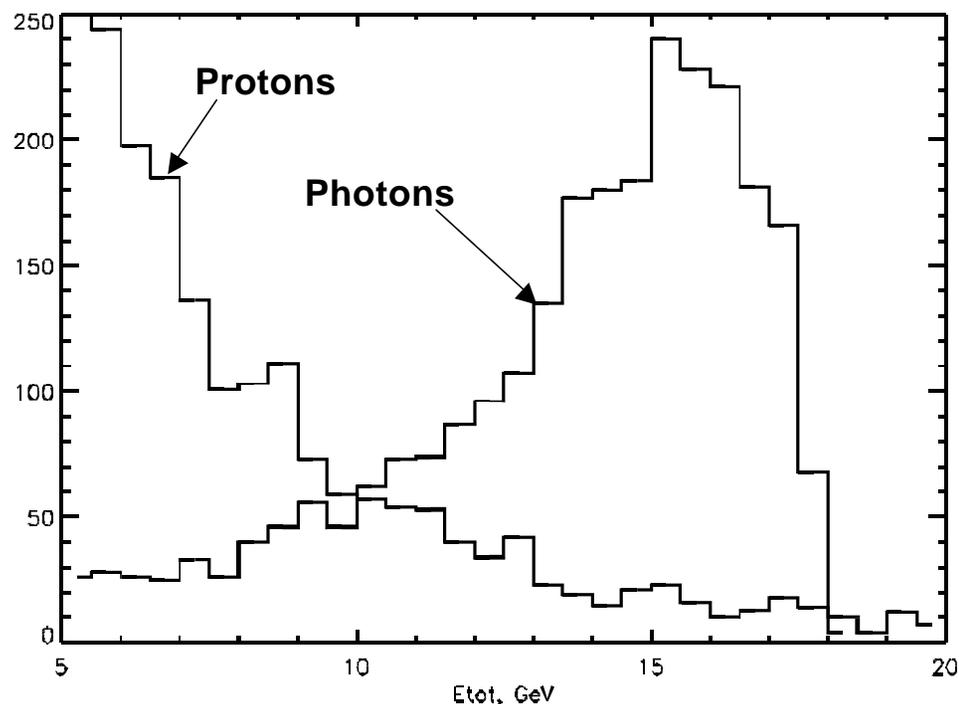


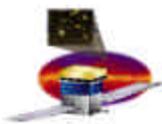
Level III- High Energy Trigger

- **High Energy Trigger:**
 - >90% efficiency for 20 GeV photons depositing at least 10 GeV
 - < 2 ms trigger latency

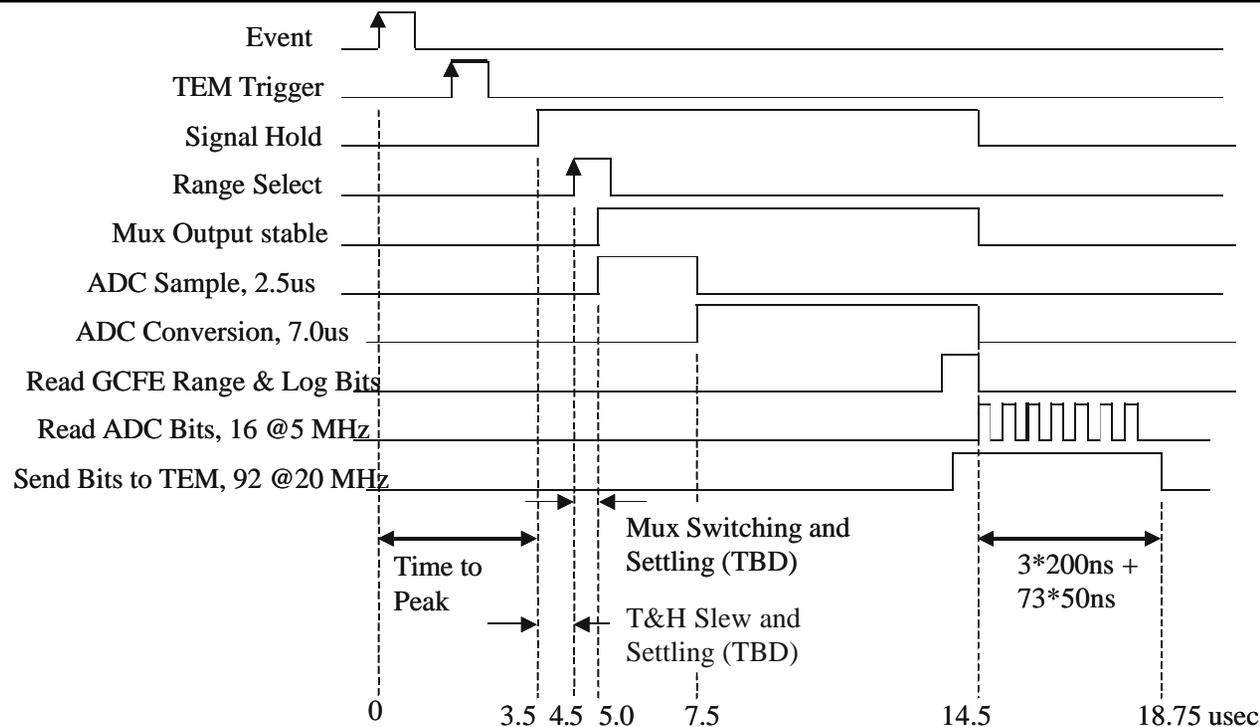
- **91% efficiency**
 - Trigger requires 3 layers in a row
 - 1000 MeV threshold
 - (from simulation)

- **< 1 ms trigger latency expected from GCFE design**





Level III-Dead Time

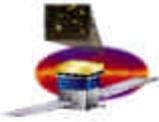


□ Dead Time

- < 100 ms per event
- < 20 ms per event (goal)

→ Achieved < 100 ms per event in BTEM99

Expect ~20 ms

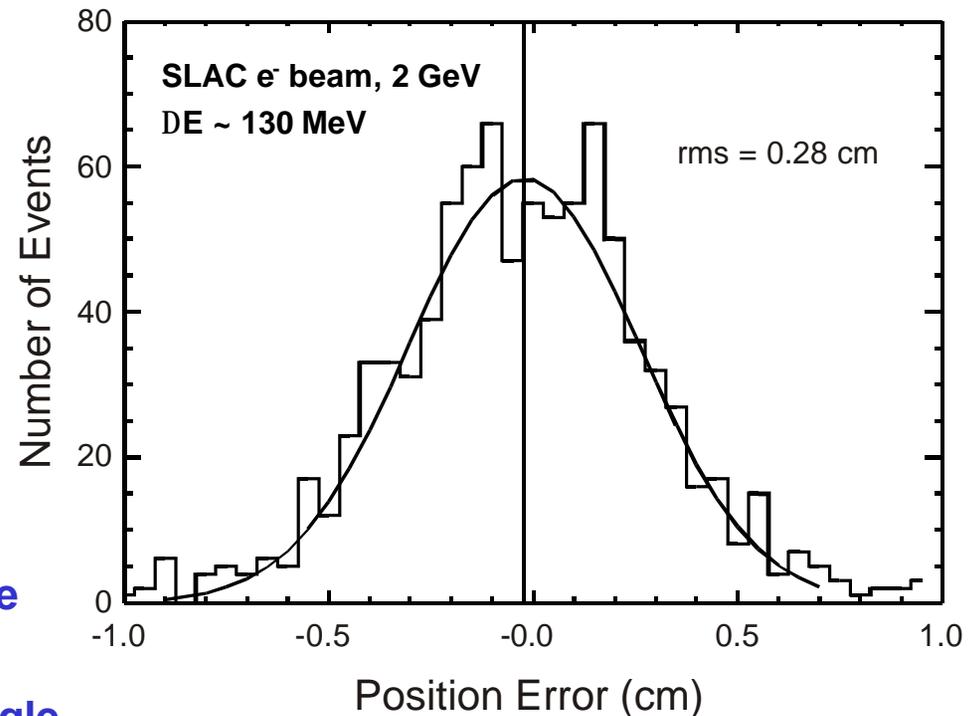


Level III- Position & Angular Resolution

- **Position Resolution:**
 - <1.5 cm in 3 dims,
min ionizing particles,
incident angle < 45 deg.

- **Cross section of crystal:**
 - 19.9 mm x 26.7 mm

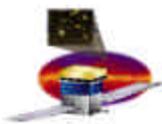
- **Longitudinal positioning:**
 - Intrinsically good
 - Limited by electronic noise
 - Expect
 - 14.9 mm @ 30 deg. angle
 - 12.2 mm @ 45 deg.



Beam Test '97 Result, 32 cm Crystal

- **Angular Resolution:**
 - 7.5 ° cos(q) deg, for cosmic
muons in 8 layers

Expect 8.1 x cos(q) deg

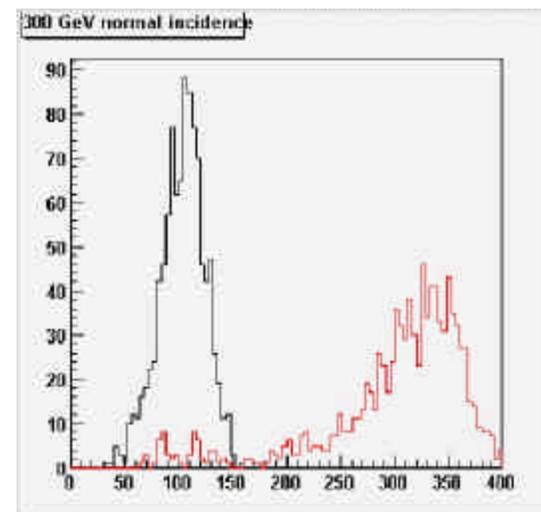
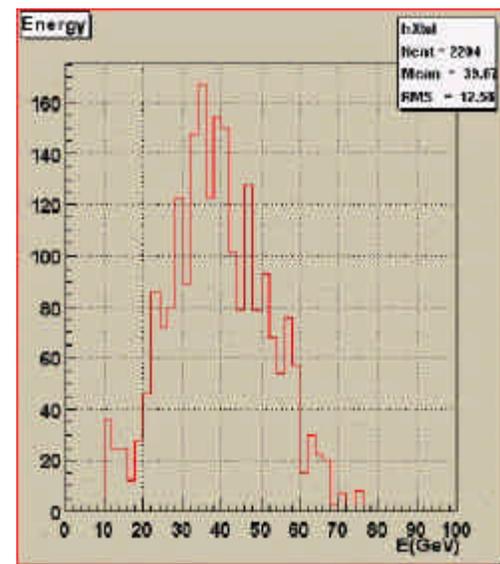


Level III-Energy Range

- Energy Range:
 - 5 MeV – 300 GeV (LAT is 20 MeV – 300 GeV)
 - 1 MeV – 1 TeV (goal)

- Low-energy end determined by electronic noise
 - Expect zero-suppress threshold @ 2 MeV (5 sigma)
 - Noise is expected at 0.4 MeV (BOL)
 - Do not want noise occupancy to significantly increase event size

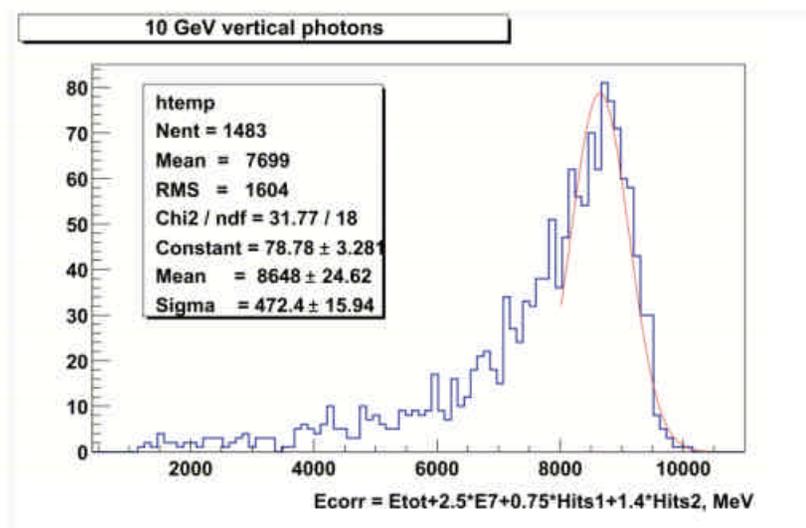
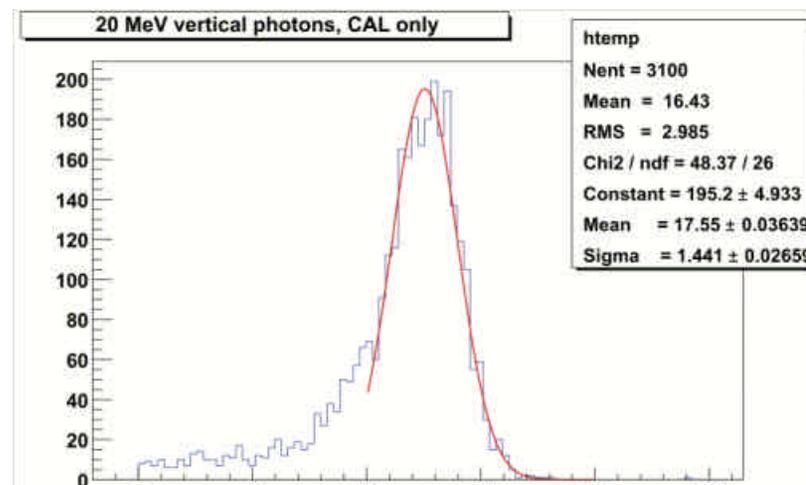
- High-energy end determined by:
 - Upper range of electronics (100 GeV /crystal)
 - Shower containment in calorimeter





Level III-Energy Resolution

- Energy Resolution:
 - < 20% (20 MeV < E < 100 MeV)
 - Calorimeter only
 - < 10% (100 MeV < E < 10 GeV)
 - < 20% (10 GeV < E < 300 GeV, on axis)
 - < 6% (10 GeV < E < 300 GeV, incidence angle > 60 deg)
- ➔ Demonstrate in simulations, beam tests
- ➔ Low-energy (20 MeV) dominated by electronic noise and ZST
- ➔ 100 MeV dominated by tracker
- ➔ 10 GeV dominated by leakage

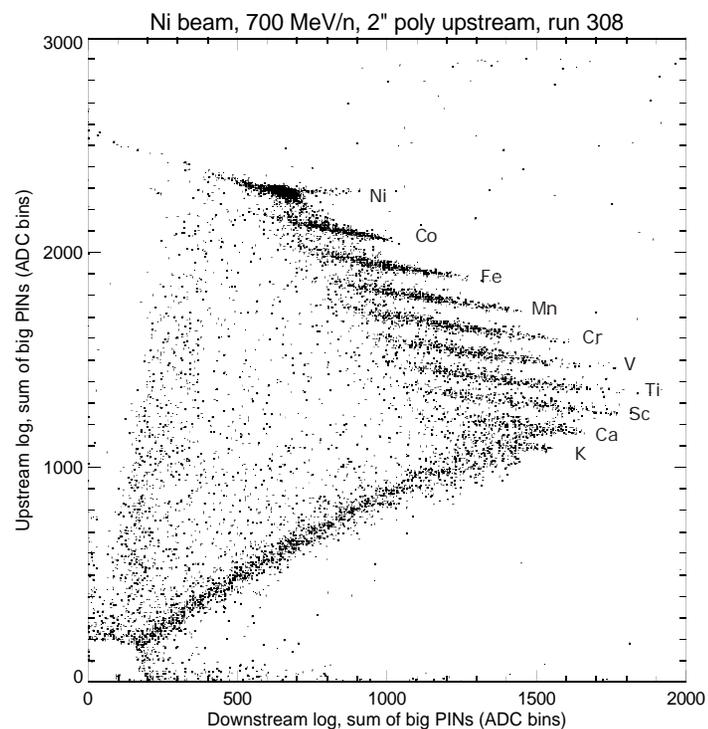
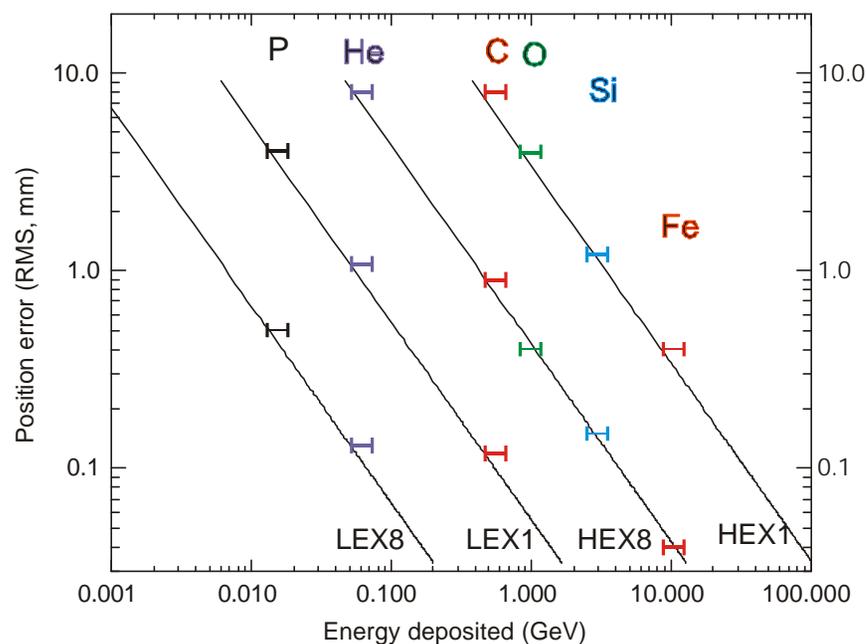




LEVEL III-On Orbit Calibration

- ❑ Relative (crystal-crystal) light yield 3%
- ❑ Absolute light yield 10%
- ➔ Demonstrated with beam tests at MSU (1998) and GSI (2000)

ADC Quantization Error & Hi-Z Cosmic Energy Depositions



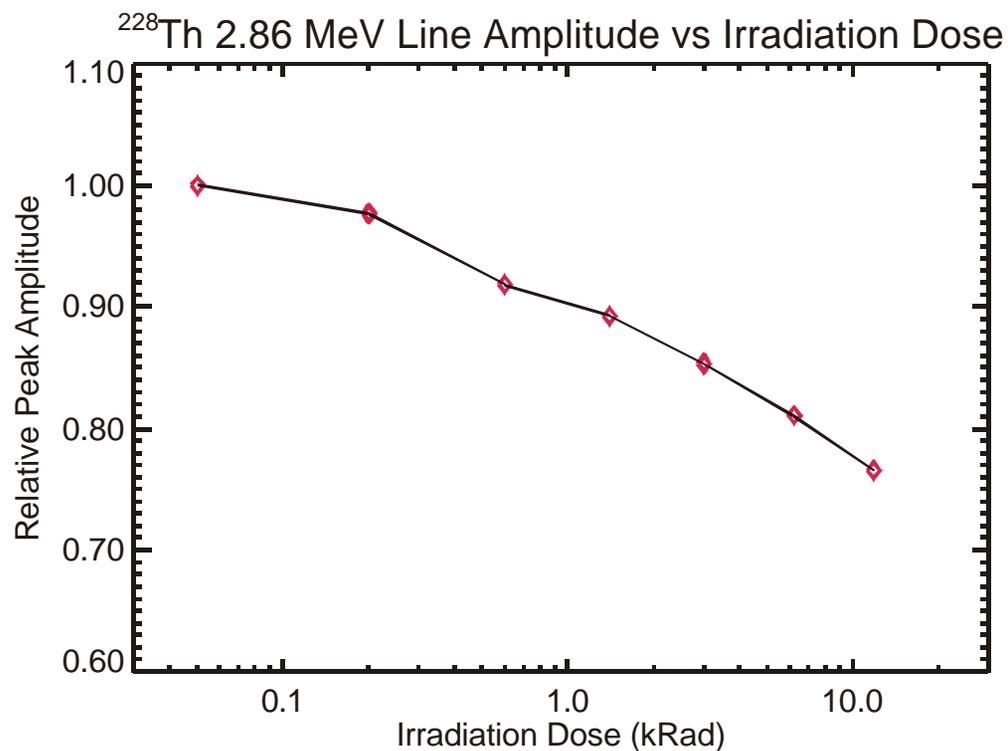


Level III-Instrument Life

- **Instrument Lifetime: >5 yrs,
with no more than 20%
degradation**

- **Most significant degradation
expected from CsI crystals**
 - Radiation causes
decrease in light yield
 - Test all CsI boules
 - Plan for loss of light yield
(gain)

- **Parts and Quality Assurance
Plan to ensure electronics will
survive**

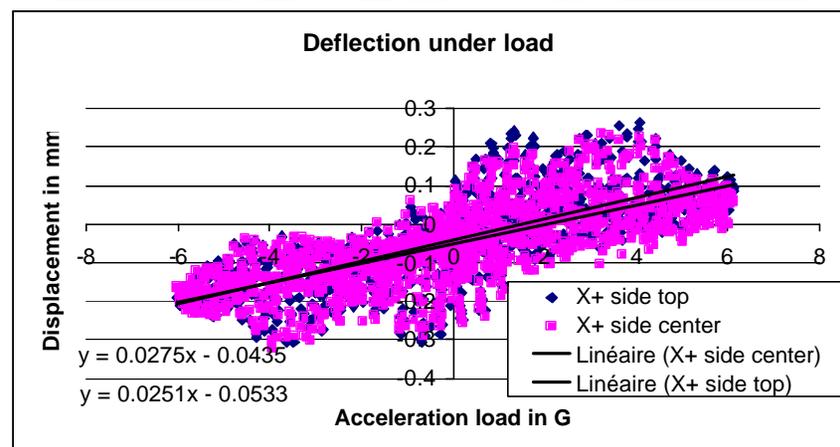
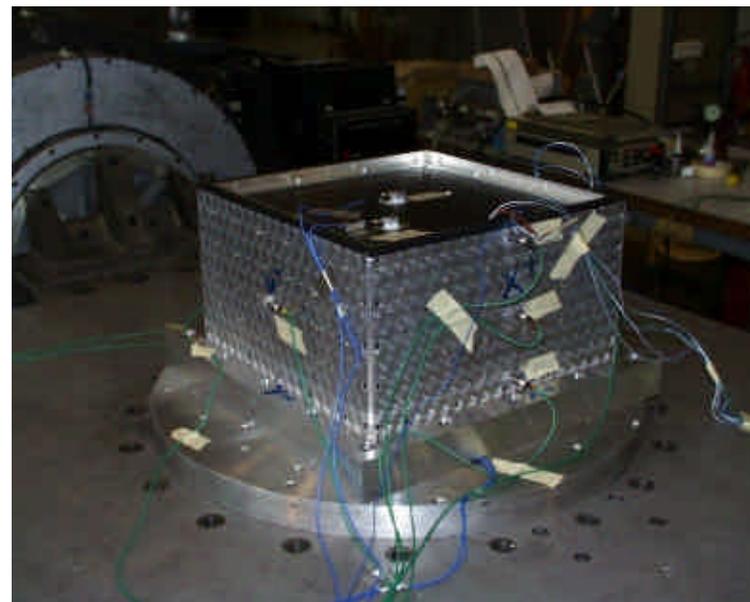




Level III- Launch Loads

- GEVS Requirements:
 - $\pm 3.5 \text{ g} / \pm 6.0 \text{ g}$ thrust static
 - $\pm 4.0 \text{ g} / \pm 0.1 \text{ g}$ lateral static

- Design
- Vibration Tests





Level III- Temperature Range

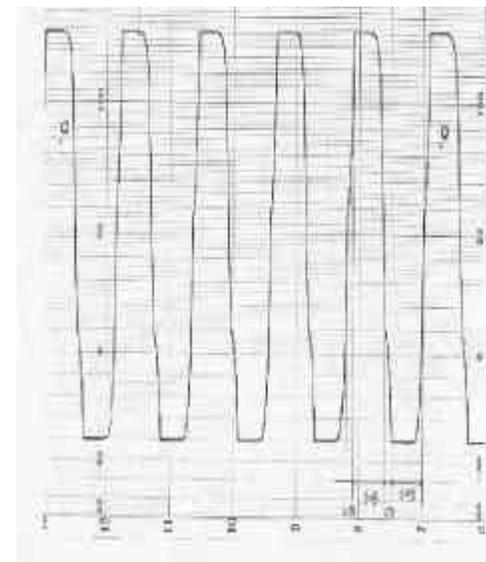
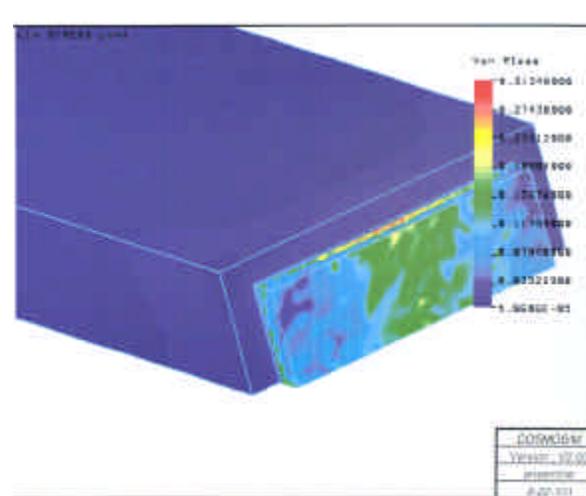
- ❑ - 10 to + 25 C operational
- ❑ - 20 to + 40 C storage, survival
- ❑ - 30 to + 50 C qualification

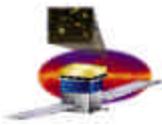
→ Design

- Large CTE of CsI
- Mechanical design allows changes in dimensions of crystals

→ Tests:

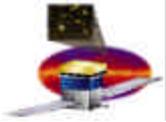
- Diodes have been tested
- Optical bond tested and selected to meet this specification





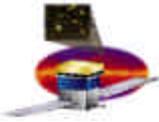
Summary

- ❑ Will meet (modified) level III requirements
- ❑ Passive material fraction could be an issue if need to reinforce bottom of grid
 - No science effect (only passive material within active volume)
- ❑ Height is close
- ❑ Temperature range big issue for CDE
- ❑ Low Energy performance known once we have ASICs
- ❑ High Energy performance demonstrated by Monte Carlo simulation



CsI Crystals

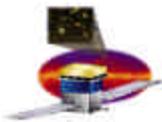
**Bernard Philips (NRL)
speaking for
GLAST Swedish Consortium**



Organization

- ❑ **Csl crystals responsibility of Swedish part of GLAST collaboration**
- ❑ **Swedish work on GLAST is undertaken by Swedish GLAST consortium**
- ❑ **PI is Per Carlson (Royal Institute of Technology, KTH)**
- ❑ **Institutions are:**
 - **Royal Institute of Technology**
 - **Stockholm University**
- ❑ **University of Kalmar contributes to the hardware effort**

- ❑ **Plan for Csl crystals:**
 - **Kalmar develops test benches/procedures**
 - **Kalmar / KTH test the crystals (mechanical / optical performance)**
 - **KTH tests boule samples (radiation harness test)**



Csl Crystals

- ❑ GLAST Calorimeter requires 96 crystals per module

- ❑ There is 1 Engineering Module planned
- ❑ There are 18 Flight Modules planned
 - 1 Qual module
 - 16 flight
 - 1 spare

- ❑ The minimal number of crystals is then 1824

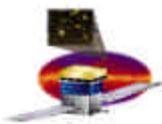
- ❑ The current plan is to purchase 2040 crystals

- ❑ Option for additional 200 crystals



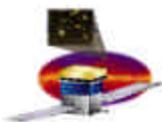
Specifications

Dimensions:	length	333.0 +0.0, -0.6 mm	at 20 C
	height	19.9 +0.0, -0.4 mm	
	width	26.7 +0.0, -0.4 mm	
Beveled Edges:	length	0.7 +/- 0.2 mm, angle	45 +/- 5 degrees
Flatness:	No point deviates from plane by > 0.2 mm		
Parallelism:	No point on opposite face deviates by > 0.2 mm from 19.7 mm, or 26.5 mm (average dimensions)		
Surfaces:	4 faces polished, 2 surfaces rough		
Light Yield:	13% FWHM (1275 keV line) at all test points, using double Tyvek + Al wrap, 11 test points evenly spaced		
Light Tapering:	Monotonic, far end is 60 +/- 10% of near end		
Radiation Hardness:	<50% with 10 kRad of Co-60		
Shipping:	shipped in groups of 12 max, < 5% humidity, sealed plastic bags		
Crystal ID:	crystal shall have serial number serial number IDs boule and location in boule		



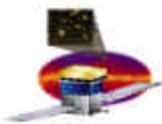
Purchase / Delivery (EM)

- Specifications written in fall 2000
- Request for bids out December 8, 2000
- Bids Closed January 22 , 2001
- 3 bids received from 2 manufacturers: Amcrys-H and Crismatec
 - Amcrys-H submitted 2 bids, direct and through French vendor
- Amcrys-H selected April, 8 2001
- Delivery for EM parts started in June 2001
- First batch (24) of crystals tested in Sweden and shipped to France
- Test equipment currently being moved to Ukraine for factory testing
- EM crystals (130) projected to be processed by end of September 2001
- All copies of test benches to be built by December 2001



First Shipment





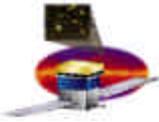
Status / Plan for QM-FM

- Purchased in same contract as EM crystals
- 1800 crystals will be delivered starting July 1, 2002
- Delivery rate is >200 crystals / month
- Dimensions for FM crystals contractually locked in March 2002
- Option for 200 more crystals
- This schedule is OK, if no holds on production

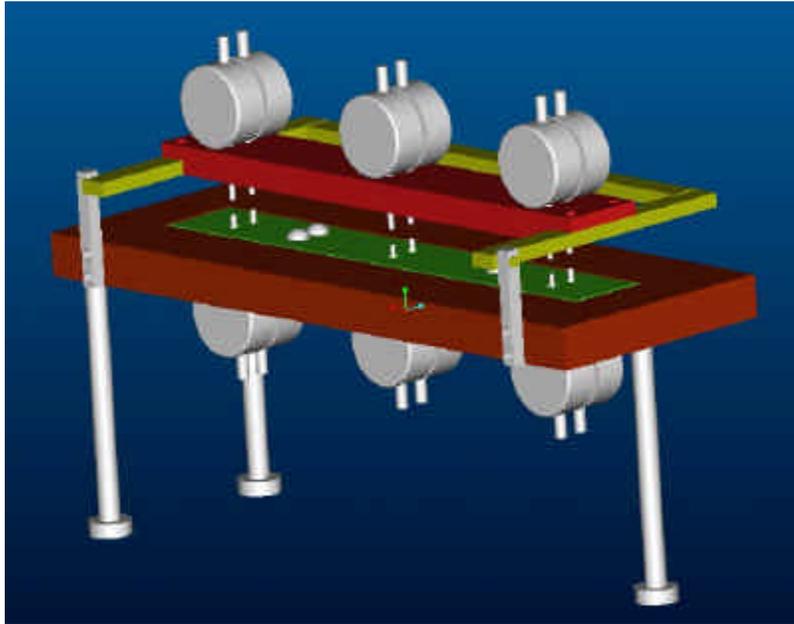


Test Procedures

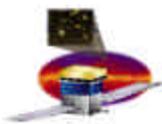
- ❑ **Measure mass of crystals**
- ❑ **Measure dimensions of crystals:**
 - **Develop mechanical test bench**
 - designed and built by Leif Nilsson of Kalmar
 - 1 test bench at factory, 1 in Sweden
 - ~ 10 minutes / crystal (Leif Nilsson)
- ❑ **Measure scintillation properties of crystals:**
 - **Develop optical test bench**
 - Designed at NRL, built at NRL (2), Sweden (4)
 - 2 test benches at factory, 2 in Sweden, 1 in France, 1 at NRL
 - ~ 1.5 hour per crystal (Georg Johansson)
- ❑ **Measure radiation hardness of crystals:**
 - **Use KTH Co-60 irradiation facility**
 - **Develop test bench (NRL,KTH)**
 - ~ few hours per sample (Mark Pearce)



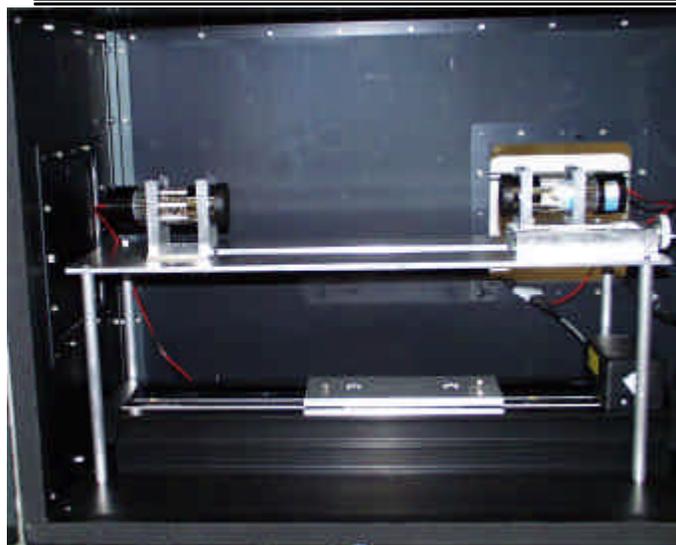
Mechanical Test Bench



- Use commercial probes
- Crystals supported on rounded pins
- Data logged into database software
- Demonstrated reliability down to 10 micron
- Export issues (Ukraine) resolved
- Use separate calipers for length measurements



Optical Test Bench



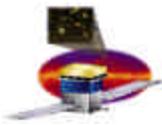
- Computer controlled slide
- Fan beam collimated Na-22 source
- Extended range PMT (2)
- Commercial NIM HV, shaping amplifiers and ADCs
- Custom interface to PC
 - Generate trigger logic
 - Programmable coincidence window
 - Put time stamp
 - Measure dead time
 - Buffer the data
 - Programmable High Voltage
- Labview control and analysis software
- First setup shipped from Sweden to Ukraine
- Second setup shipped from NRL to Sweden
- Other 4 setups ready by January 2002



Radiation Testing

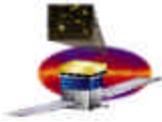


- ❑ Can provide 0.5 kRad/min
- ❑ Samples are 2.54 cm Diam. X
2.54 cm Height
- ❑ Will use commercial PIN diode
 - Same spectral response
- ❑ Use hybrid preamplifiers
- ❑ Use commercial NIM
shaping amplifiers/ADCs
- ❑ Measure light loss with
Cs-137 source (662 keV)



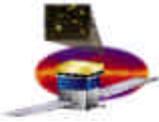
Summary

- Financing for Swedish consortium in place**
- Specifications for Csl crystals exist**
- Contract for all crystals in place**
- Test equipment built and tested**
- Test equipment being shipped to factory**
- Deliveries have started**
- First batch of crystals tested**
 - **Light yields good**
 - **Light tapering good (mostly)**
 - **Crystal cross section good (dimensions, flatness and parallelism)**
 - **Crystal length on high side (correct for temperature)**
- First batch of crystals shipped to France**
- Do not expect problem meeting schedule or specifications**



Calorimeter Modules Mechanical and Thermal Design

Oscar Ferreira
Mechanical Engineering Group
LPNHE Ecole Polytechnique



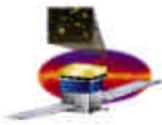
Requirements: Environmental

□ Launch loads: static loads

LAT INSTRUMENT PRIMARY	Event	
	Liftoff / Transonic	MECO
Thrust axis	+3.25 g / -0.8 g	+6.0 ±0.6 g
Lateral axis	±4.0 g	±0.1 g
Load factor	1.25 for qualification levels	

□ Launch loads: random vibrations

CAL MODULE	Acceleration Spectral Density	
	Qualification	Acceptance
20 Hz	0.01 g ² /Hz	0.01 g ² /Hz
20 – 50 Hz	+4.55 dB/Oct	+2.28 dB/Oct
50 – 800 Hz	0.04 g ² /Hz	0.02 g ² /Hz
800 – 2000 Hz	-4.55 dB/Oct	-2.28 dB/Oct
2000 Hz	0.01 g ² /Hz	0.01
Overall Level	7.63 gRMS	5.65 gRMS



Requirements: Environmental (2)

Launch loads: Other

- **Acoustic noise**

Structure shall guaranty that full functionality is preserved after acoustic noise levels as defined in LAT Mechanical performance Specification. Minor effect is expected due to compactness and mass of the CAL modules

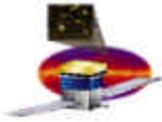
- **Shock loads**

Mechanical structure shall preserve full functionality of CAL module under piroshock loads defined in LAT Mechanical performance Specification

- **Depressurization**

CAL module shall withstand time of rate of pressure as define in LAT Mechanical performance Specification

No air shall be trapped inside the cells, venting path shall allow gazes to exit at the base of the CAL modules

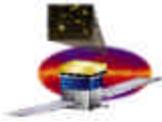


Requirements: Environmental (3)

□ Environmental thermal loads

CAL MODULE	Event	
	Operational	Survival
T min	-10 °C	-20 °C
T max	+25 °C	+40 °C
Rate of change	5 °C/hour max	

On orbit heat flux non applicable, CAL module enclosed inside grid bays



Requirements: Functionality

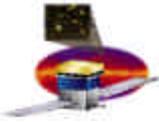
Mass and Geometry

□ Mass

- Mass of mechanical structure shall be less than 12 kg per module

□ Outer dimensions

- Stay clear dimension for CAL module:
 - Transverse: 364 x 364 mm²
 - Height: 224 mm (15 for the attachment tabs)
- 9x9 mm² chamfer in the corners of the module



Requirements: Functionality (2)

Strength and Stiffness

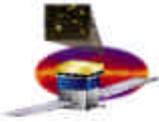
❑ Max allowed displacements

CAL MODULE	Max allowed displacements		
	Transverse	Thrust	
		Base	Top
Static loads	0.5 mm	0.25 mm	0.5 mm
Random vibration	0.25 mm	0.25 mm	0.5 mm
Natural frequency	First natural frequency of module > 100 Hz		

❑ Values are defined for qualification levels
❑ Displacements values are point to point values
❑ For random, values indicated are RMS values

❑ Stiffening of grid

- The base plate of the CAL shall have the equivalent stiffness of at least a 8 mm thick solid aluminum plate



Requirements: Functionality (3)

Thermal control

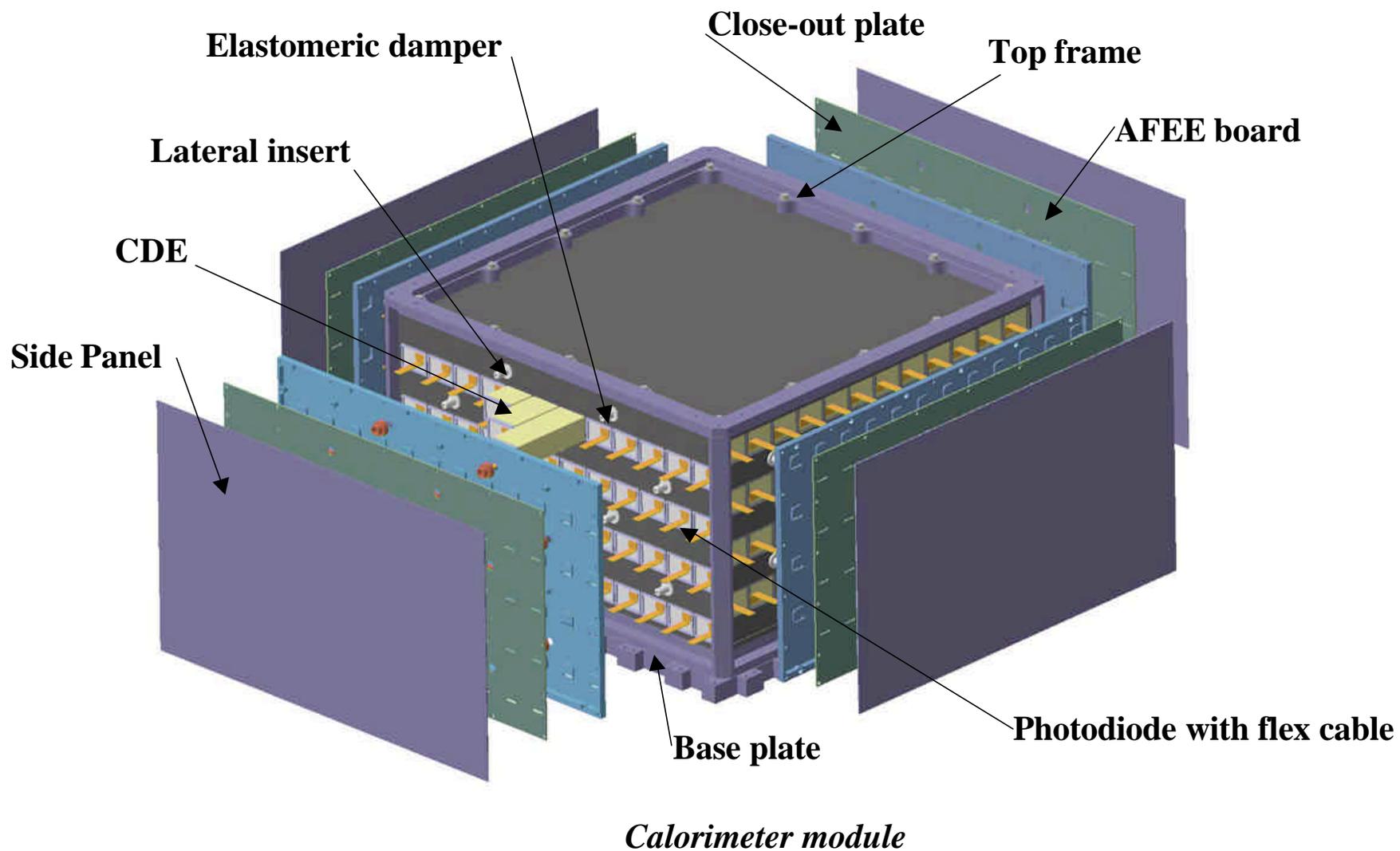
No active cooling on the CAL modules, heat dissipated by the AFEE boards and electronic boxes attached below the modules need to be transferred into the grid through the attachment tabs

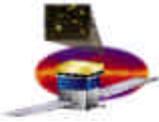
- Thermal control of electronic boxes
 - Temperature gradient between interface with grid and interface with electronic boxes shall be less than 5 °C

- Thermal control of AFEE boards
 - Temperature gradient of the boards shall be less than 5 °C
 - Temperature raise in AFEE boards due to power dissipated by electronic boxes shall be less than 3 °C



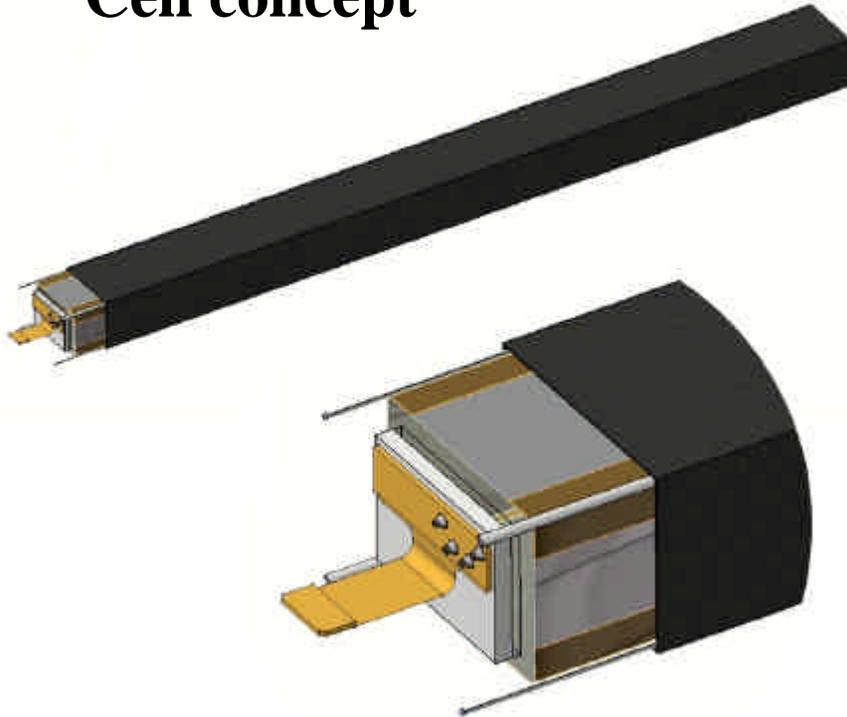
Design





Design Concept

Cell concept



CDE inside GFRP cell

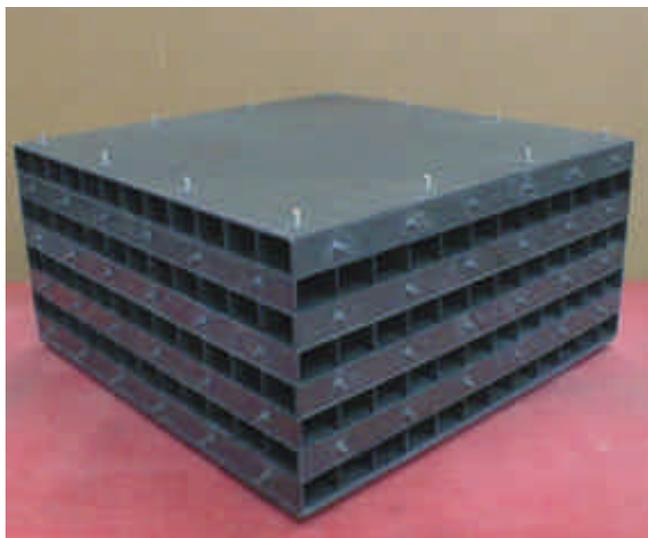
- **Stiff envelop around each CDE able to withstand environmental loads without requiring contribution from the logs**
 - **Design does not rely on poor mechanical properties of Csl**
 - **Accuracy of mech. structure is independent of tolerances of logs**
 - **Access is granted to any log, independently**



Design Concept (2)

Structure concept

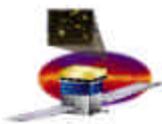
- ❑ Structure manufactured as a single part from GFRP material, 96 cells with X-Y layout
- ❑ Metallic inserts integrated inside the composite for attachment of mechanical parts



Structure for VM1 model

Composite Structure	Dimensions	
	Nominal	Tolerances
Transverse	340x340 mm ²	0 / -0.2
Height	176.8	0 / -0.2
Vertical pitch	27.84 mm	±0.05
Horiz. pitch	21.35 mm	±0.05
Cell transverse	27.35x20.5 mm ²	0 / -0.04
Cell length	340 mm	0 / -0.2

Composite Structure	Thickness of composite walls	
	Nominal	Tolerances
Top wall	2.4 mm	±0.1
Base wall	4.4 mm	±0.1
Side wall	1.7 mm	±0.1
Inner vertical	0.36 mm	±0.04
Inner horiz.	0.72 mm	±0.04



Materials

Composite Structure	
GFRP structure	Graphite epoxy composite
Side insert	Ti-6Al-4V Titanium alloy
Top insert	Ti-6Al-4V Titanium alloy
Bottom insert	Ti-6Al-4V Titanium alloy
Structure shell	
Top frame	2618A Aluminum alloy
Bottom plate	2618A Aluminum alloy
X side close-out plate	2618A Aluminum alloy
Y side close-out plate	2618A Aluminum alloy
Corner	2618A Aluminum alloy
Spacer	2618A Aluminum alloy
X side panel	5754 Aluminum alloy
Y side panel	5754 Aluminum alloy
Dampers	
Damper elastomer	RTV Silicone
Damper frame	2618A Aluminum alloy
Elastomeric cord	Silicone

- **Fabric**

TORAY T300 3K 0° / 90° 193 g/m²

Thickness of laminate 0.18 mm

- **Choice of composite material**

- **Need to meet out-gassing requirements**
- **Low curing temperature to preserve compatibility with 3M mirror film (constraint released)**
- **High strength graphite fibers preferred to high modulus to allow small radius of curvature**

- **Resin system**

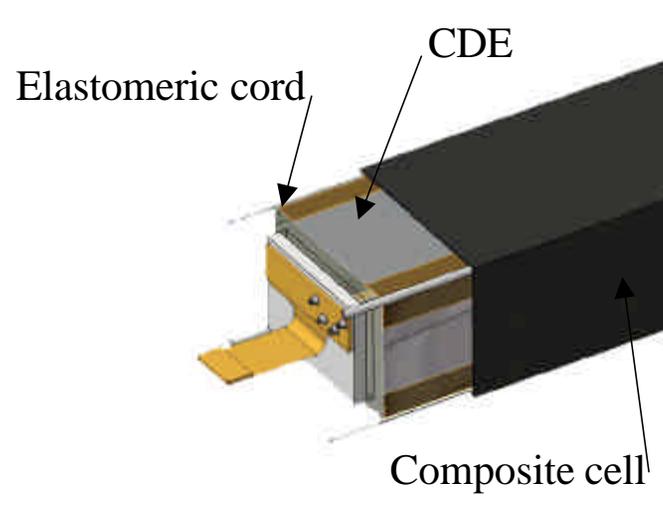
M10 epoxy matrix, curing temperature 120 °C
alternatively, for better out-gassing properties
M76 epoxy, curing temperature 135 °C
Both products from HEXCEL COMPOSITES



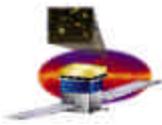
Interface with CDE

CDE Transverse support

- ❑ Clearance between cell and Csl log for assembly, 0.3 to 0.5 mm per side, related to crystal tolerances
- ❑ Silicone elastomeric cords to wedge the CDE
- ❑ Cords stretched to provide room for assembly, released to provide support
- ❑ f1 mm cords guaranty support in any configuration
- ❑ » 400 % elongation needed to reduce the diameter to 0.5 mm, for assembly



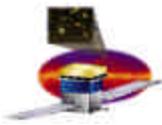
CDE	Room in cell corners for elastomeric cords	
	Clearance min	Clearance max
Chamfer min	0.55 mm	0.75 mm
Chamfer max	0.75 mm	0.95 mm



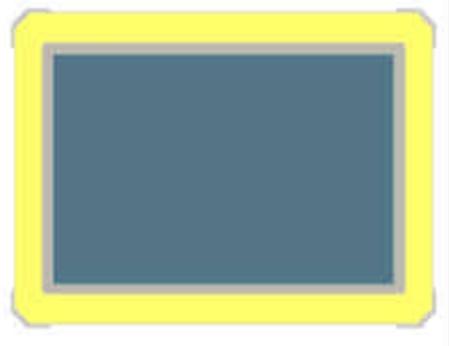
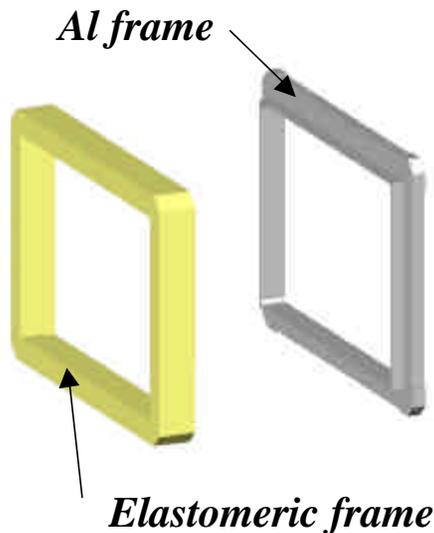
Interface with CDE (2)

CDE: longitudinal stop

- ❑ **Conflicting requirements:**
 - **Expansion of the logs shall not be constrained**
 - **For 20 °C to 50 °C temperature range expansion is 0.54 mm**
 - **Longitudinal motion of log shall be minimized**
 - **Maximum allowed displacement 0.5 mm to keep safety margin between the top of the photodiode and the close-out plate**
- ❑ **Elastomeric damper at the end of the logs to provide soft stop and allow thermal expansion**
 - **Shape and durometer optimized to allow at least a 0.2 mm expansion at both ends of the logs and keep stress levels in the logs below 0.5 MPa.**
 - **Displacement of log under 12G acceleration below 0.3 mm**



Interface with CDE (3)



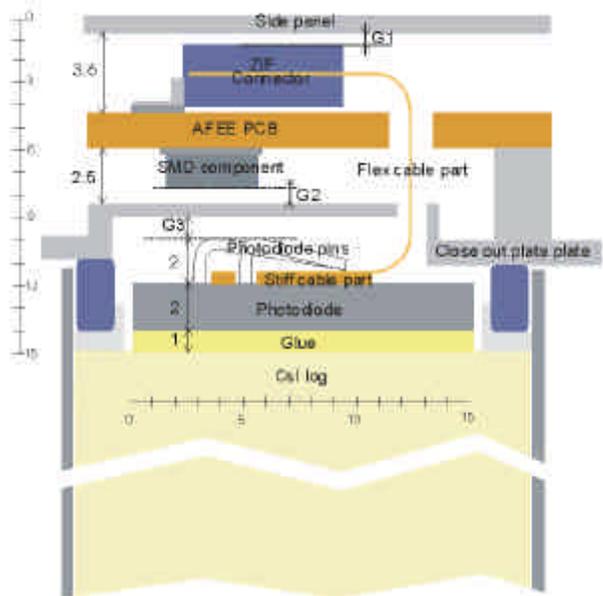
- ❑ Damper for CDE ends: Silicone elastomer attached to an aluminum frame,
 - Al frame adjusted inside composite cell with 0.1 mm or less gap
 - Step on frame edge to allow venting of air trapped inside the cell
 - Flange between elastomer and photodiode to prevent stress on bonding during lateral expansion of the elastomer

- ❑ Gap between photodiode and Al frame is kept at 0.5 mm to guaranty that no contact with the photodiodes is possible during transverse displacements of the CDE
 - Thickness of elastomeric damper 1.5 mm (height 3 mm)

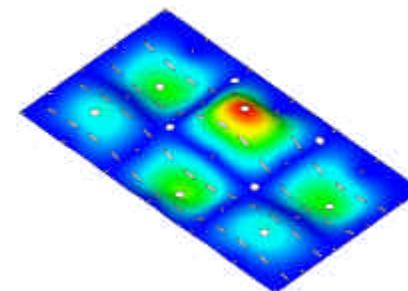
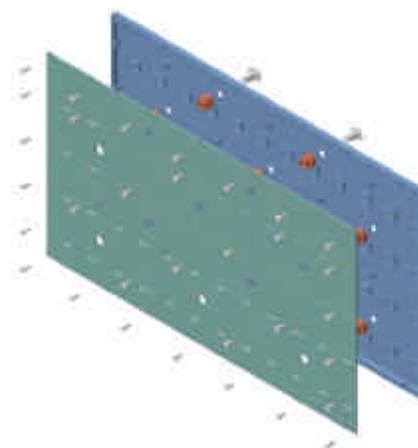


Interface with AFEE

- ❑ Boards attached to the close-out plates, on a stiffening frame and bosses to maximize available area for components
 - Deformation of the boards follows deformation of the module: 0.5 mm
- ❑ Flex cables cross close-out plate and boards
- ❑ Bosses to escape photodiodes pins
- ❑ PC Boards are enclosed between the close-out plates and side panels for efficient shielding



Gap between components and plates in mm			
	Min	Ave.	Max
Side panel - connector	0.45	0.75	1.05
Close-out - SMD component	0.5	0.85	1.2
Photodiode – closeout boss	0.8	1.5	2.3



First mode 976 Hz

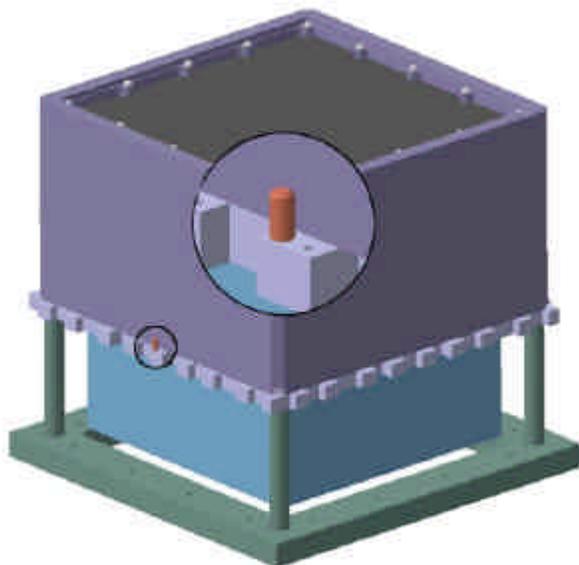


Interface with grid

□ Interface with the grid

The interface with grid is provided by the CAL base plate. It ensures:

- Structural and thermal interface
- Alignment of the modules
- Stiffening of the base of the grid



□ Integration inside grid bays

– Alignment between CAL modules

- The top of the tabs of base plate defines the contact plane
- 1 Reference pin attached to the base plate defines the position in plane
- 1 Reference pin attached to the base plate defines the orientation in plane

Tolerances budget

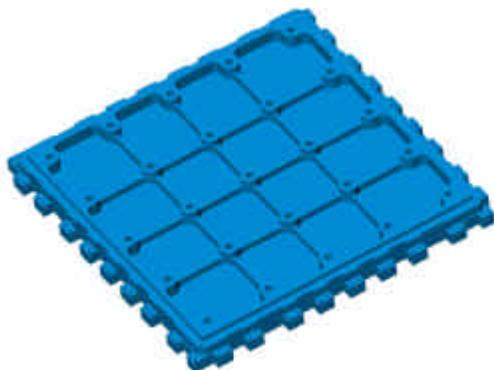
CAL outer dimensions: 363 mm 0 / -0.4	
Alignment of pins	0.05 mm
Perpendicularity of sides	0.25 mm
Symmetry (shift)	0.2 mm
Total per side	0.5 mm
Stay clear dimensions: 364 mm	



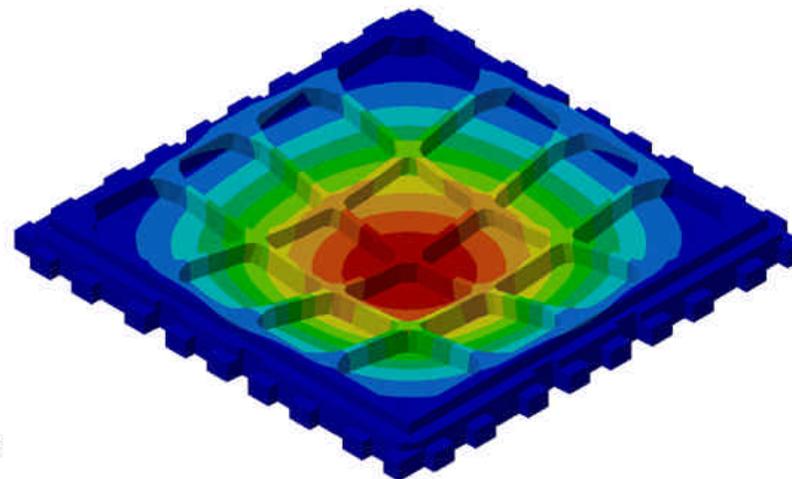
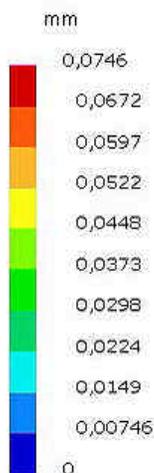
Interface with grid (2)

Base plate stiffness

- ❑ Design of base plate modified to include a 6 mm thick solid part to provide stiffness to the grid
 - Provides equivalent stiffness of 10 mm thick plate
- ❑ Optimization of material distribution is in progress to reduce weight (< 4 kg in present design)



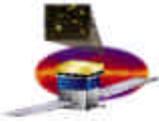
Displacements Iso



Flexion under 10000 N load

Comparison to solid 10mm thick plate: Displacements (10000 N load)

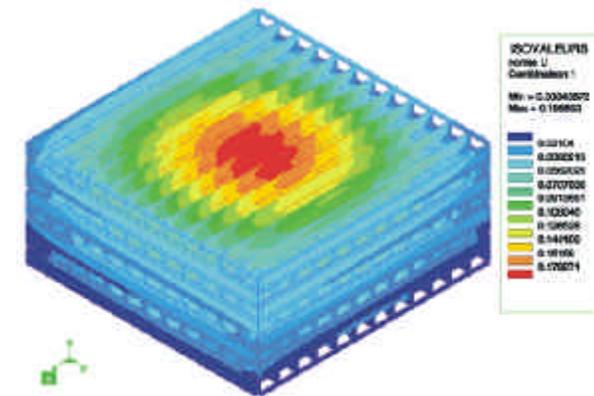
	Base plate	Solid 10 mm
Traction	0.012 mm	0.020
Shear	0.040 mm	0.070
Flexion	0.075mm	0.110 mm



Structural Performance

Static

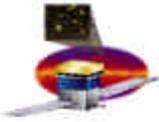
Max static displacements		
	FE Analysis	VM1 sine burst test
Transverse: 5g	0.14 mm	0.16 mm
Thrust: 8.25g	0.12 mm	0.18 mm



Deformation under 12 g thrust

Results from analyses predict stiffer structure than measurements on VM1: the influence of stiffness of the close-outs of the cells needs to be improved on the model

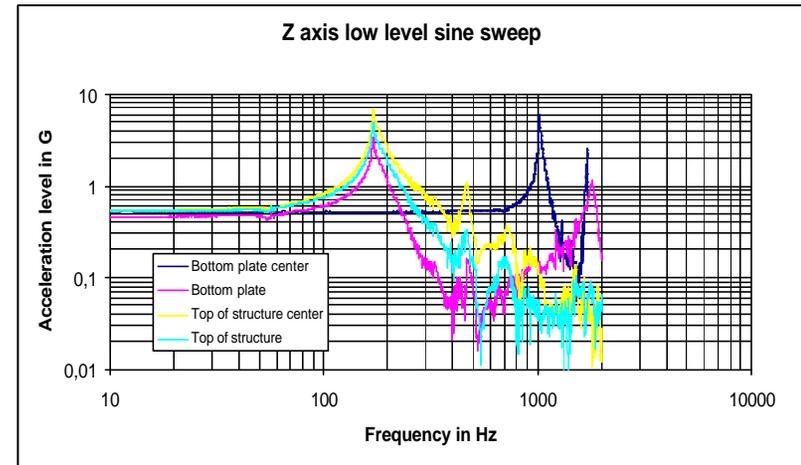
Both analysis and test show comfortable safety margin to max allowed displacement: 0.5 mm



Structural Performance (2)

Natural frequencies

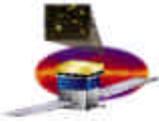
- Natural frequencies measured with VM1 shake test
 - Transverse, flexion: 115Hz Q=6
 - Thrust, drum mode: 175 Hz Q=10



Results from VM1 sine sweep: thrust axis

Frequencies from analysis for VM2	
Frequency	Deformation
246 Hz	Flexion mode X
258 Hz	Flexion mode Y
273 Hz	Drum mode
311 Hz	Torsion mode

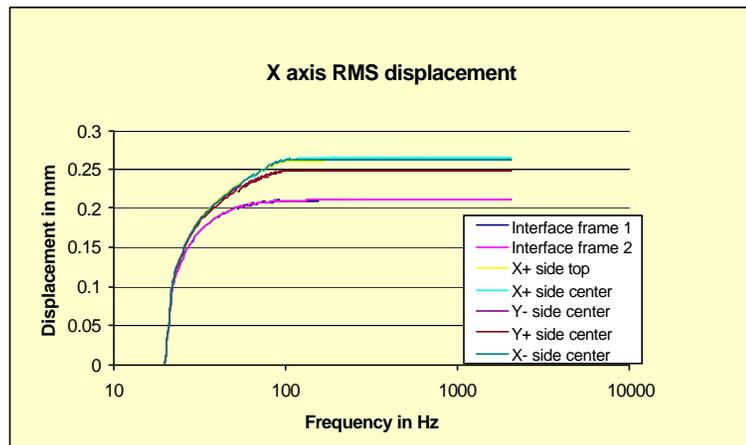
- Analysis predicts improved performance for VM2 and EM models, mainly for transverse frequency. Stiffer close-out plates improve shear strength of the structure



Structural Performance (3)

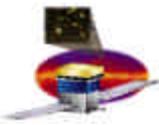
Random vibrations

- Performance of mechanical structure under random vibration have been measured on VM1 model with qualification levels. Detailed information is available in documents LAT-TD-269 and LAT-TD-243



RMS displacement for transverse vibrations

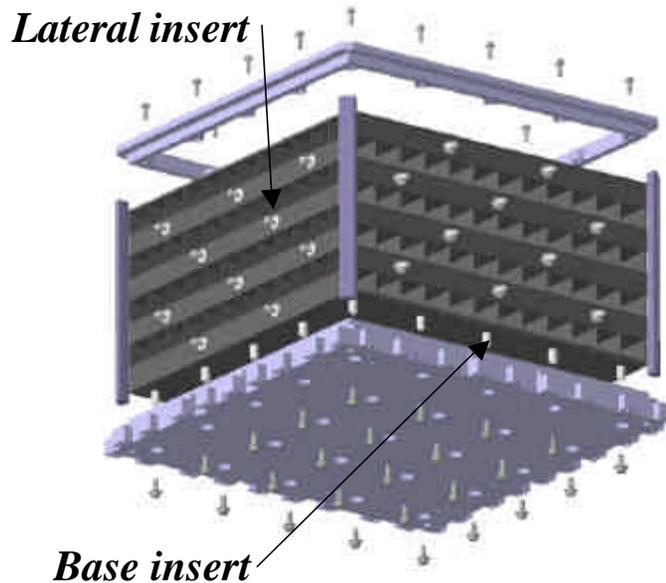
Max point to point displacement under random vibrations	
Transverse	0.47 mm
Thrust top	0.77 mm
Thrust bottom	0.45 mm
3s values, assuming maximum measured acceleration level applied on the full model	



Structural Performance (4)

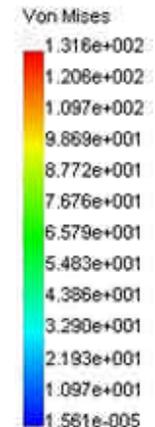
Inserts

- The GFRP structure is attached to the Al shell by inserts. Stress levels on the inserts will result from different load events
 - Static and dynamic environmental loads
 - Load due to thermal expansion of logs
 - Load due to CTE mismatch between Aluminum parts and GFRP

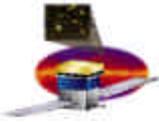


Stress levels evaluated with local models

VonMises Equivalent stress		
	Lateral insert	Base insert
CTE mismatch	135 MPa	43 MPa
Env. Load	23.5 MPa	5.5 MPa



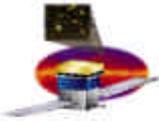
Stress levels in lateral inserts due to CTE mismatch



Thermal Control

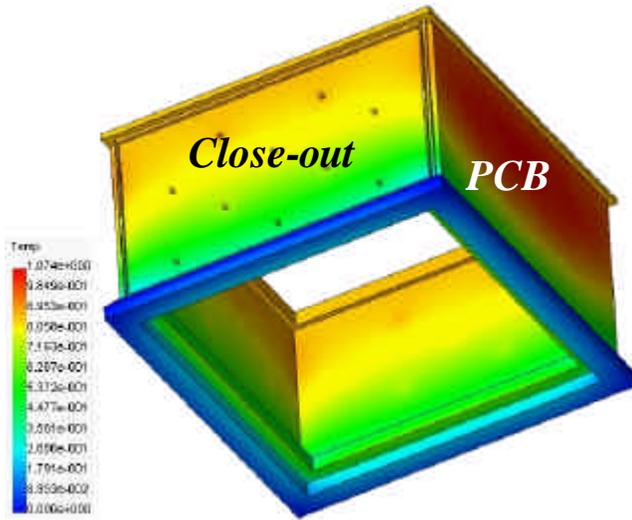
- Regulated temperature at the top of the grid: power dissipated by the AFEE boards and electronic boxes transferred through the tabs of the base plate
 - Heat path for AFEE boards
 - PCB => Close-out plates => Base plate => Grid webs
 - Total power » 1 W per board
 - Heat path for electronic boxes
 - Chassis => Base plate => Grid webs
 - Max power 50 W (TBR)

- CsI logs offer a high thermal mass but are insulated inside the cells. Their thermal inertia does not help in regulating the temperature of the modules



Thermal Control (2)

$$DT < 1.2 \text{ }^\circ\text{C}$$



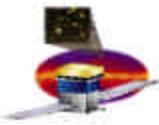
Temperature profile

Thermal conductivity of PCB for model

In plane: $K_x = K_y = 100 \text{ W}/(\text{m}^\circ\text{K})$

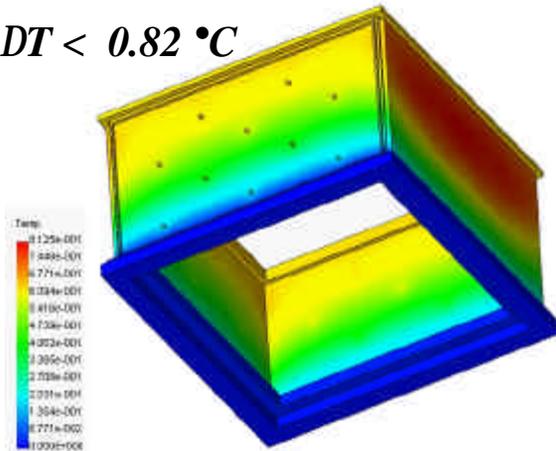
Perpendicular: $K_z = 0.8 \text{ W}/(\text{m}^\circ\text{K})$

- ❑ Heat power dissipated by the boards is low 1W and evenly distributed on the surface of the boards
- ❑ Good thermal exchange surface with the close out plates on the perimeter of the boards and bosses.
- ❑ CAL base plate acts as a thermal barrier between the AFE boards and the electronic boxes attached below the modules
- ❑ Main temperature gradient is expected at the interfaces between the elements
 - Good surface finishing of aluminum parts
 - Surface treatment to preserve thermal contact characteristics: chromate conversion treatment ALODINE 1200



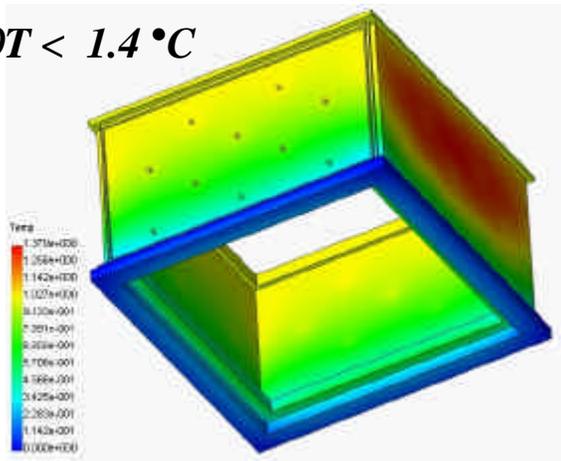
Thermal Control (3)

$DT < 0.82\text{ }^{\circ}\text{C}$



Temperature profile without electronic boxes

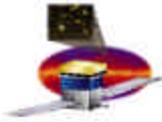
$DT < 1.4\text{ }^{\circ}\text{C}$



Temperature profile with $K=50\text{ W}/(\text{m}\cdot\text{K})$

Analysis

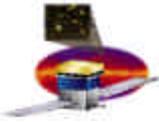
- Simplified FE model built to detect possible design flaws
 - Includes aluminum structure and PCBs
 - thermal contact resistance of bolted joint not included
- Temperature raise in AFEE due to power supplies and TEM boxes limited $\gg 0.5\text{ }^{\circ}\text{C}$
- Influence of thermal conductivity of PC board limited, bosses help in regulating the temperature in case of low conductivity



Thermal Control (4)

- ❑ **Analysis needs to be improved and completed**
 - **More detailed geometrical FE model**
 - **Analysis of thermal contact resistance and integration into the model**
 - **Transient analysis, evaluation of Csl contribution**

- ❑ **Thermal tests planed on VM2 to validate concept and adjust model**
 - **Require dummy PCB**
 - **Require heat source below the base plate**



Manufacturing

Mechanical parts manufacturing

- ❑ Aluminum shell (close-out, side panels...) and base plate production shared between industry and in-house fabrication

- ❑ Parts of the tooling for the manufacturing of the composite structure produced in the industry

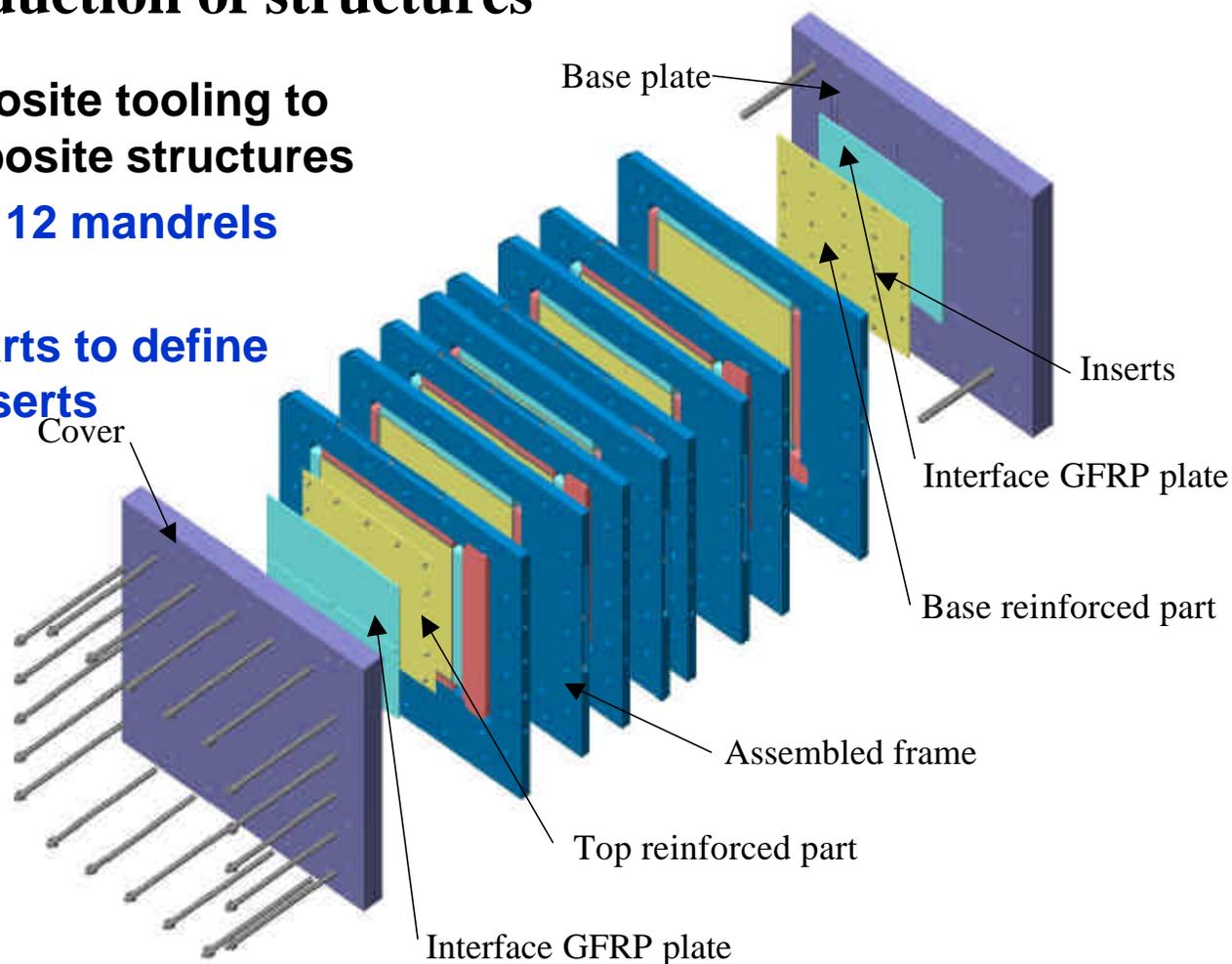
- ❑ In house production for GFRP structures
 - All design, developments and prototypes manufactured in house
 - Production performed by the technicians involved in the developments
 - Equipment available
 - Workload fits with group capacity and availability

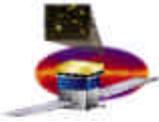


Manufacturing (2)

Tooling for production of structures

- Aluminum - composite tooling to produce the composite structures
 - 8 frames with 12 mandrels each
 - Composite parts to define position of inserts



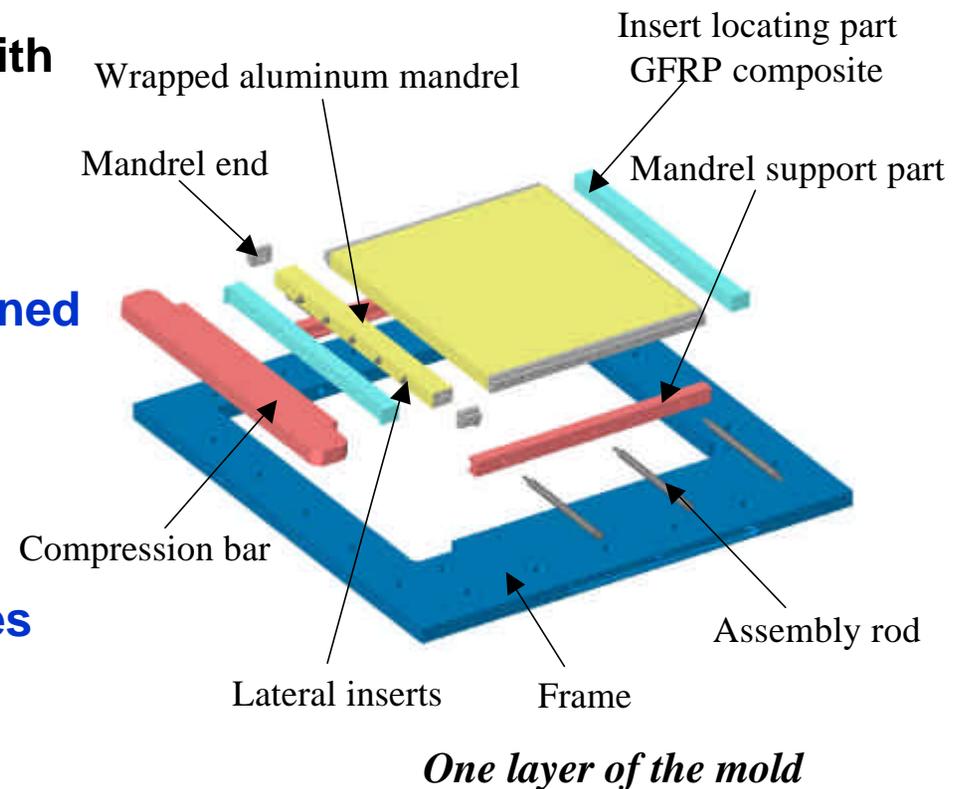


Manufacturing (3)

□ Dimensions of parts corrected to take into account CTE mismatch between the tooling and the structure: geometry is defined at epoxy curing temperature

□ All mechanical part machined with tight tolerances

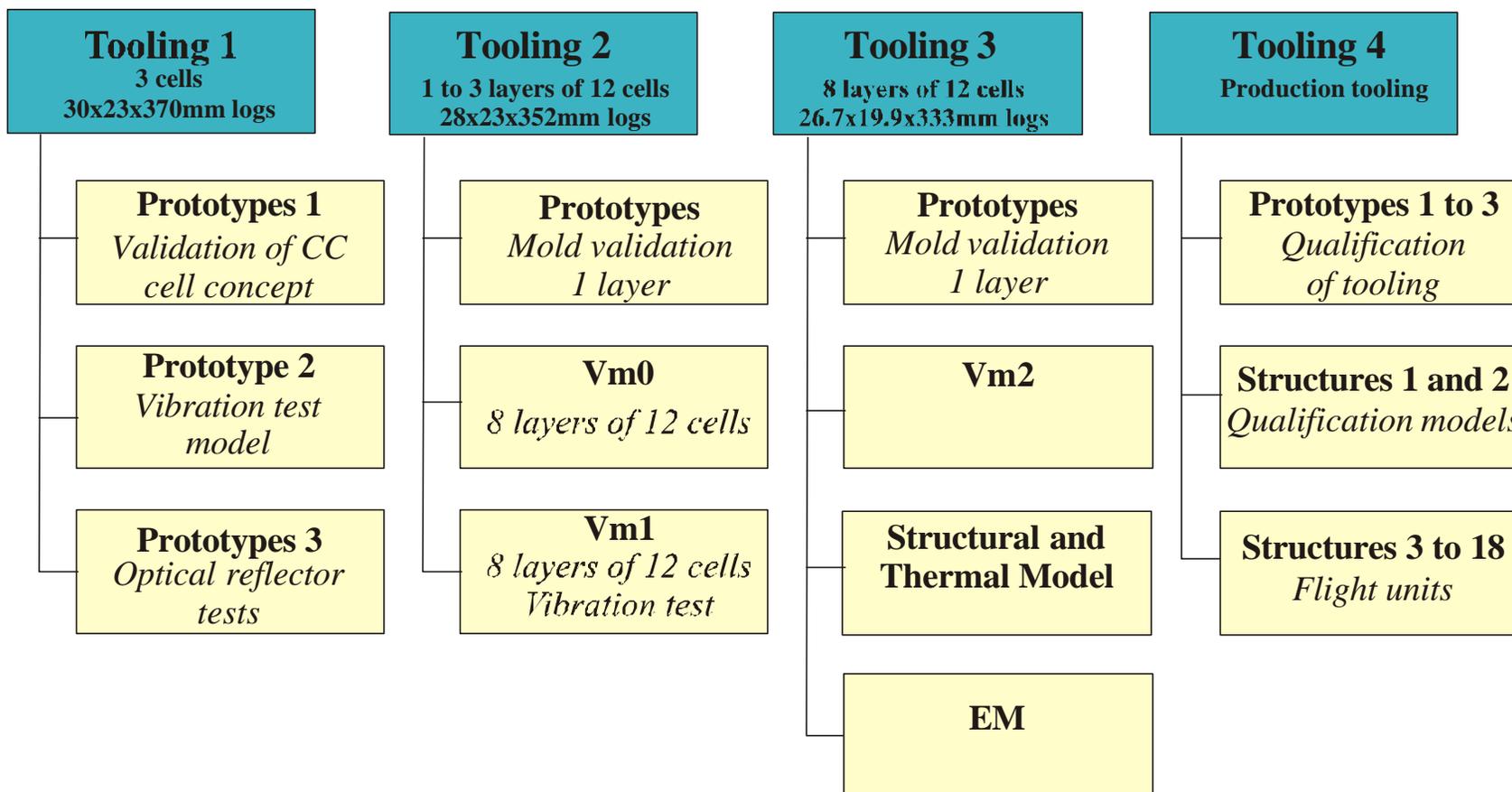
- ± 0.02 mm for aluminum mandrels
- Transverse dimensions defined by aluminum frame
- Height defined by stack of frames
- Alignment pins to ensure relative positioning of frames

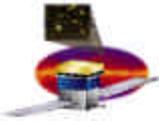




Developments

□ Tooling and corresponding prototypes and models





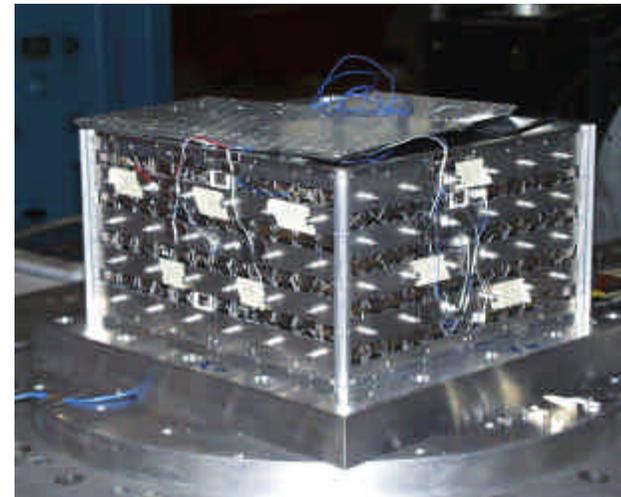
Developments: VM1



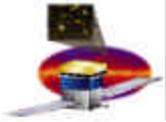
Insertion of dummy logs inside VM1

- ❑ Complete composite structure: 3 parts assembled
- ❑ Configuration with all the mechanical parts but not final design
- ❑ Cells filled with 93 steel dummy logs and 3 CsI logs (no wrapping)

- **Successfully passed shake test with qualification levels with no degradation of optical performance of crystals**
 - Sine sweep
 - Random
 - Sine burst



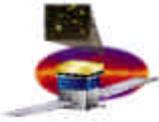
Instrumentation for shake test



Developments: VM2

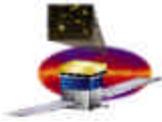
- ❑ **Currently under development**
 - **Final dimensions**
 - **Tooling to produce a 96 cell composite structure**
 - **All parts already machined, verification tests about to start**
 - **Aluminum mechanical parts integrate all interface constraints**
 - **Equipped with 12 CDE**

- ❑ **Science performance evaluation before LAT PDR**
- ❑ **Environmental tests and thermo-mechanical tests before EM to allow possible design adjustments**



Summary of Requirements

Requirements	Validated			Remarks, actions
	Yes	No	Part.	
Mass of structure <12 Kg	x			Checked with design, needs to be measured on VM2 and EM
Dimensions, tolerances			x	Extrapolation from performance achieved on prototypes, needs to be measured on VM2
Strength, static	x			From VM1 sine burst test, to be updated on VM2
Natural frequency >100 Hz	x			Measured with VM1 shake test, needs to be updated with improved VM2 design
Random vibrations	x			Performance evaluated with VM1 shake test, needs to be updated on VM2
CDE transverse support			x	Validated with Csl logs without wrapping and photodiodes
CDE longitudinal stop		x		No relevant information from VM1 shake test, need dedicated evaluation
Thermal control of PCBs			x	Rough analysis done, needs improvement Will be tested on VM2
Assembly of CDE inside cells	x			Tested with several prototypes and, in particular, VM1



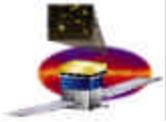
Issues and Concerns

❑ Issues

- Structural analysis of CAL modules needs to be improved and completed, particularly thermo-mechanical analysis is missing
 - A subcontractor has been chosen to perform the study. Work will start in September. It will cover analysis of the CTE mismatch between materials, design of the inserts. Tests will follow.
- Shake tests have been successfully performed with Csl logs but no test with CDE has been done so far
 - A shake test with one cell equipped with a CDE in the current design configuration is planned before instrument PDR

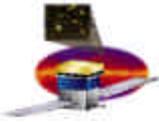
❑ Concerns

- A lot of handling of the Csl logs is needed for assembly and test. Even if the procedures are followed, a risk to deform the logs remains with such a soft material.
- Time is short between PDR and CDR and between CDR and first delivery date. Production of the mold for the structures and of parts needs to start before CDR.



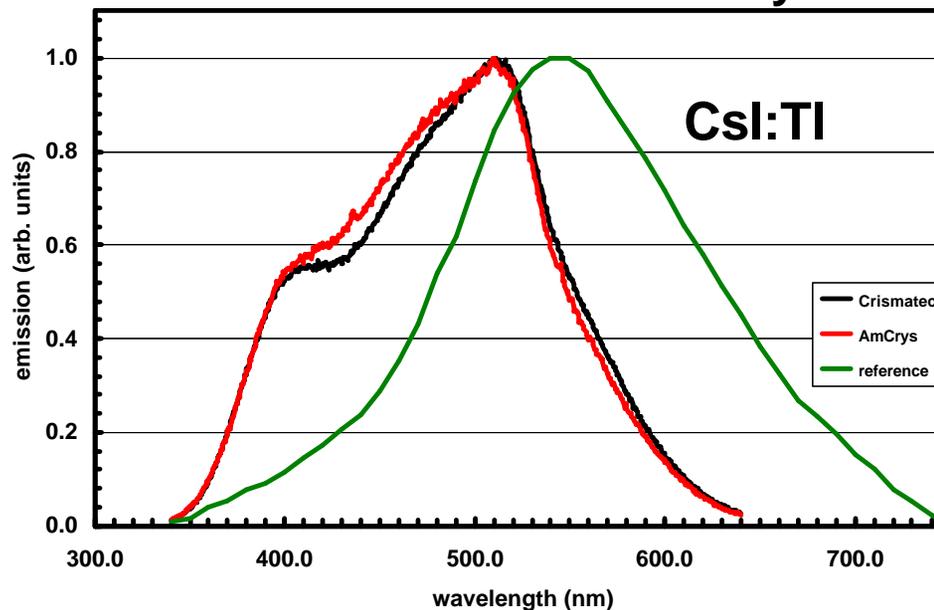
LAT Calorimeter Crystal Detector Element (CDE)

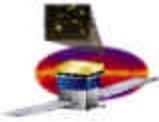
Didier Bédérède
CEA Saclay



CDE Concept

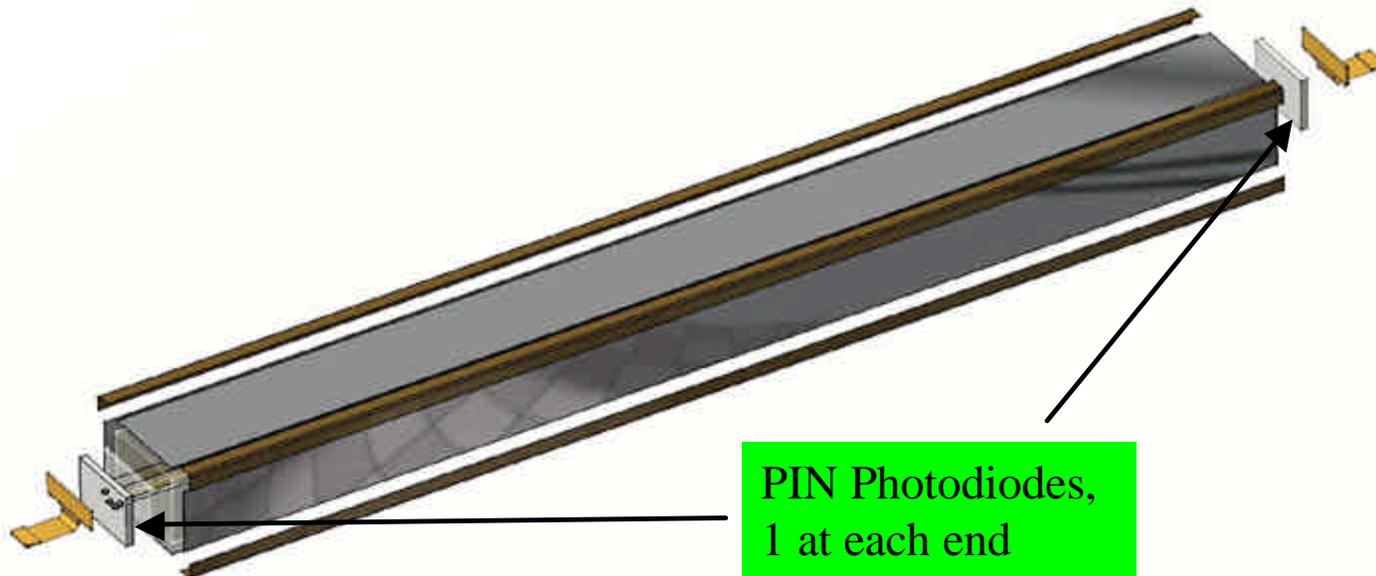
- ❑ The Crystal Detector Element uses the scintillation properties of the Crystal of Cesium Iodide doped Thallium : when charged particle (coming from interaction of Gamma ray with matter) cross the crystal it deposits energy transformed by scintillation in visible light transformed by photodiode in current.
- ❑ Hereafter a comparison between scintillation (green) of literature and photoluminescence measured from Amcrys and Crismatec crystals



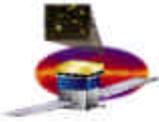


CDE Concept

- The emitted light is recovered by PIN photodiode (sensible to visible light) at each end of the crystal.
 - Summing signals of both ends allow a reconstructing of deposited energy.
 - The difference in the two ends provides measure of interaction point along the length of the crystal

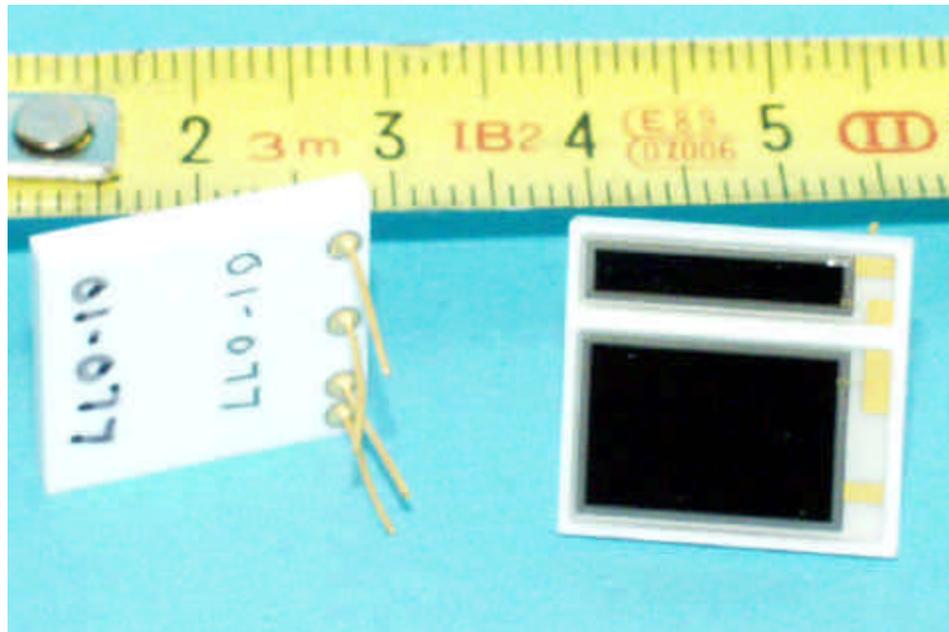


PIN Photodiodes,
1 at each end

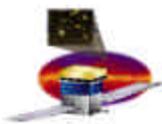


CDE concept : Dual PIN Photodiode

- ❑ To be able to read the large dynamic range ($\sim 10^5$), the gamma energy is divided in two paths. So readout is performed by two PIN Diodes potted in the same ceramic carrier.
- ❑ A flex cable recovers the signal from the DUAL PIN DIODES (DPD)

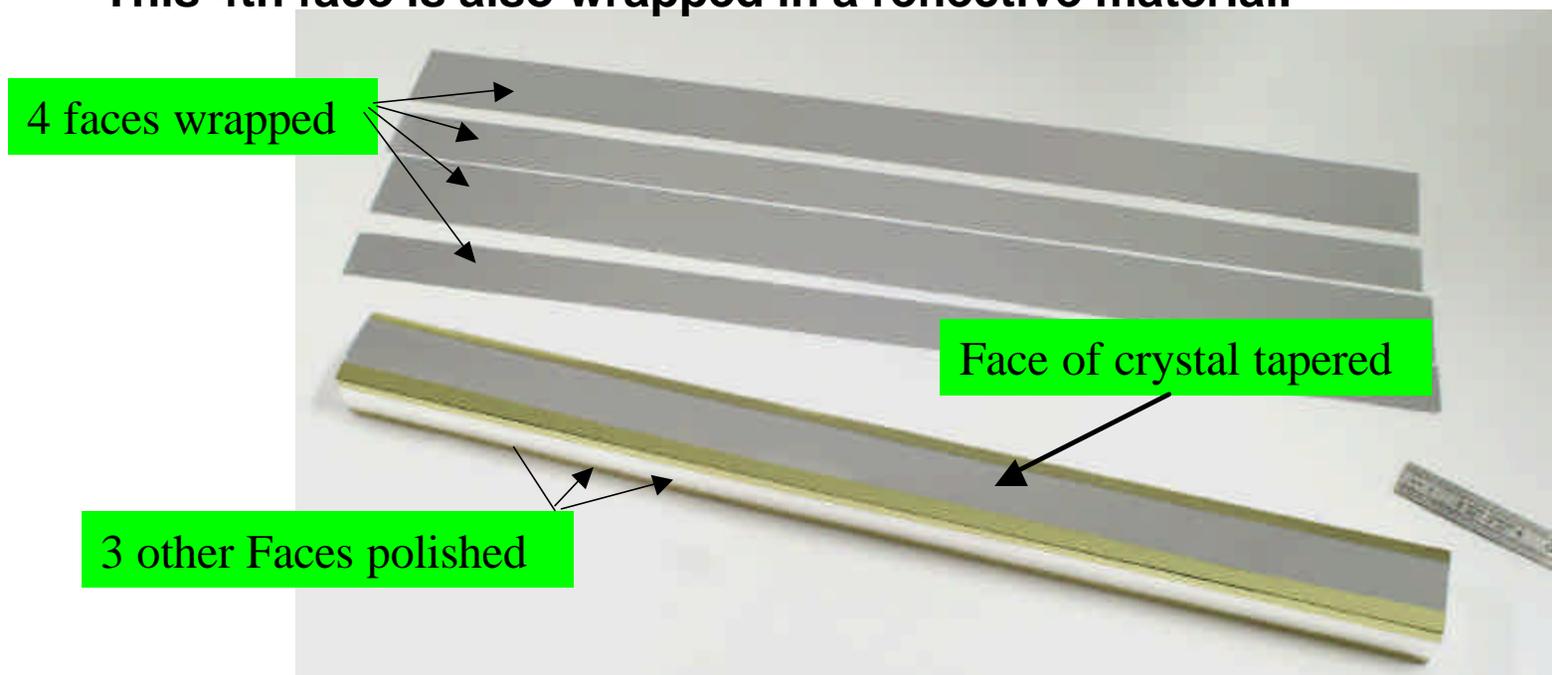


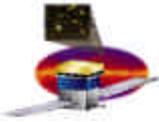
Dual Diode concept –
96 mm² and 25 mm²
prototype from Beam
Test EM calorimeter



CDE Concept (Crystal+wrapping)

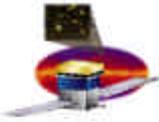
- ❑ Crystal is polished on 3 faces and wrapped in a reflective material to prevent light losses.
- ❑ To be able to measure the position of the impact of particles in the crystal with a resolution of 1mm the crystal is tapered on the 4th surface (Differences signals of both ends allow to know the position). This 4th face is also wrapped in a reflective material.



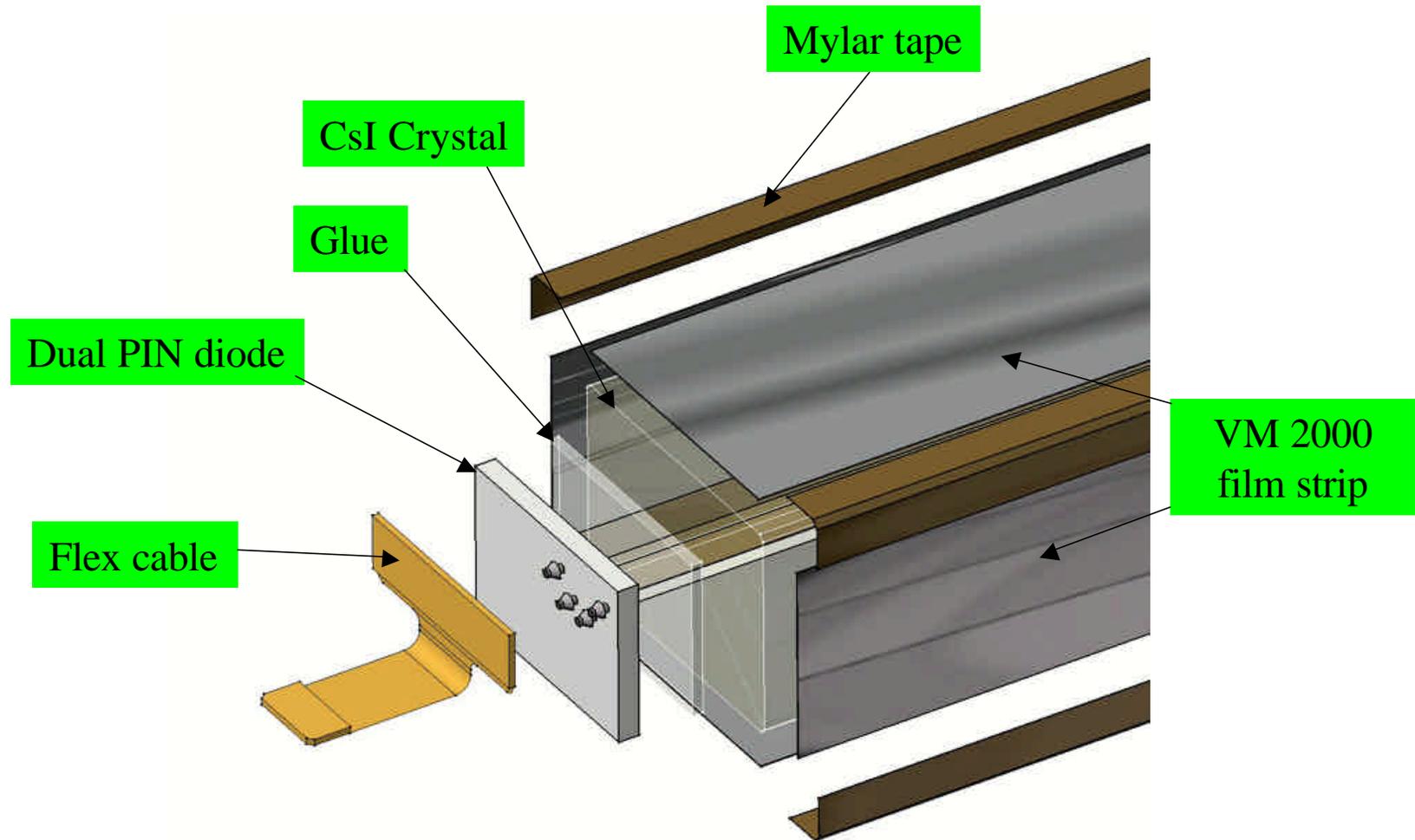


CDE Requirements

		min	max	For Area A		For Area B	
				min	max	min	max
CDE	Lightyield (e/MeV)			800	—	5000	—
	CDE width (mm)	26,4	26,8				
	CDE length (mm)	340,5	342,1				
	CDE height (mm)	19,6	20,0				
Xtal	See Csl crystals (B.Philips)						
Wrapping	Reflectivity	89 %	—				
DPD	Sensitive area of Photodiodes (mm*mm)			10,5* 2,4	—	10,5* 14,5	—
	Photodiode quantum efficiency (A/W)- 540 nm			0,33	0,41	0,33	0,41
	Dark current nA			—	3	—	10
	Capacitance pF			—	15	—	100
DPD & flex	Capacitance				15		100
Bonding DPD&flex on Xtal	Optical coupling transparency	95%	100%				
	Optical Coupling index Csl/DPD	1.41	1.8				
Environm ent tests	Vacuum Thermal cycling (100)	-30°C	+50°C				

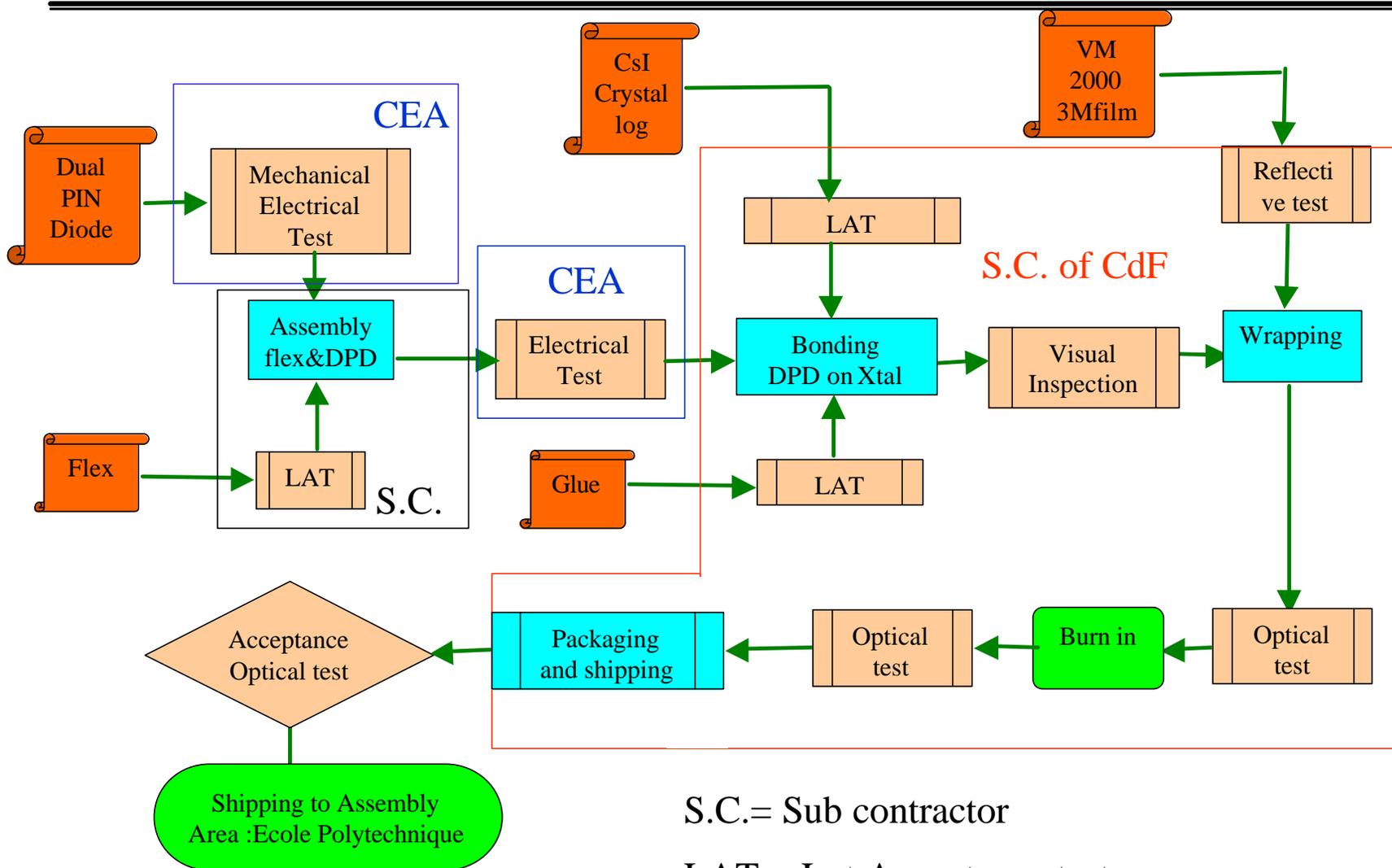


Crystal Detector Element (Wrapped) End





FM CDE Flow chart



S.C.= Sub contractor

LAT = Lot Acceptance test



Dual PIN Diodes delivery and plan

□ VM2+EM production

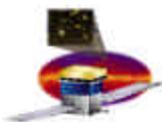
- 100 diodes final dimensions (Hamamatsu) to NRL on 08/15/2001.
- 200 diodes final dimensions (Hamamatsu) and some ceramic carrier will come to CEA (France) on 9 September 2001.
- Kapton flex cable will be attached by space subcontractor.

□ Tests

- Electrical (each) and optical receipt (samples) tests are performed on naked diode. Isolation tests performed on diode + flex.
- Some diodes + ceramic carrier + flex attachment will go through qualification tests
- VM2 24 diodes (with flex) are bonded to 12 crystals
- EM 192 diodes (with flex) are bonded to 96 crystals

□ QM+FM production with a call for tender

- Hamamatsu is able to manufacture (with two product lines) 600 pieces per 5 weeks. This is not a concern to reach planning.
- 100 pieces can be attached per week. This meets schedule.



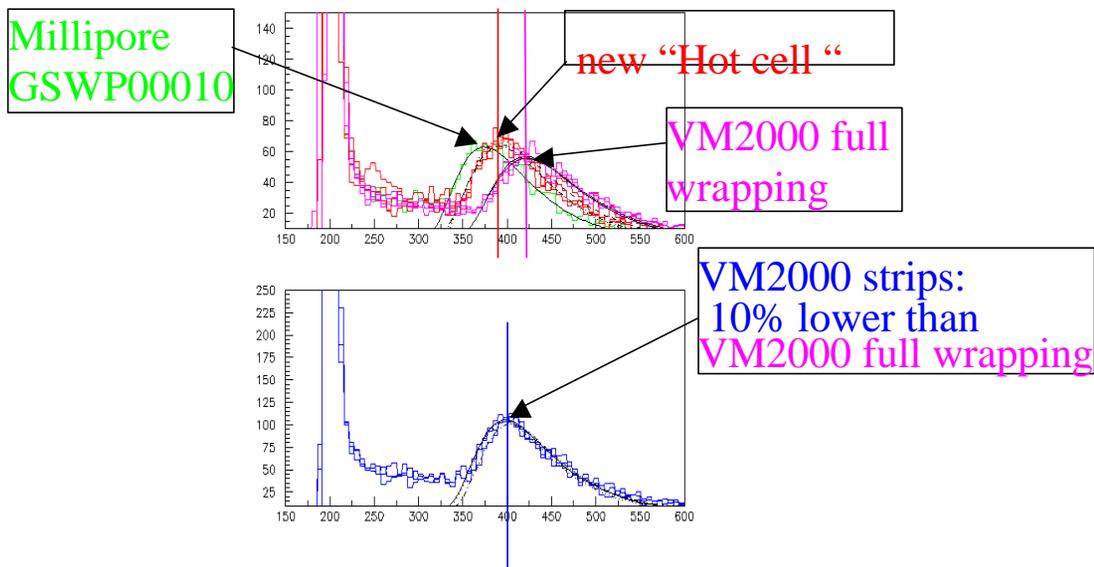
Wrapping Options

VM2000 strips	Hot cell	Wrapping and place in a carbon cell (Baseline)	Remarks
Structure	Molded with the carbon fiber structure	Cut to dimension of each face of the crystal. Tape on the beveled edges	Additional tooling for cold cell
Lightyield	>5000 e/MeV big diode	10% more than hot cell	
CDE test before insertion	No light yield test is possible	The CDE is well known before insertion	Hot cell mixes functions mechanical and optical. A degrade optical cell induce to reject the whole structure
Crystal protection during vibrations lateral	Proven on VM1	Must be better than hot cell (envelope protection)	
Crystal protection during vibrations longitudinal	Proven on VM1	identical	Crystal held the same way



Light Yield vs Wrapping Options

Same Crismatec crystal, 28 x 19.6 x 352



□ VM2000 strip solution

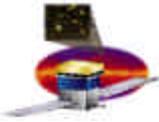
- Roll of VM 2000 are standard manufacturing from 3M.
- Strips must be chosen in foil which offers a reflectivity better than 89%
- Cut the foil into strips (laser cutting is foreseen)
- Mylar tape is a spatial tape easily available



Thermal Simulation of Bonding to CsI

- Thermal (-30°,20°) simulation of constraints on different glues curing at 20°C by CETIM

	Masterbond EP29 Hard epoxy	Masterbond EP37 3FLF Soft epoxy	Dow corning 93500 with primer
E(tensile modulus)	2600 MPa	490 MPa	?
Tensile strength	45 MPa	28 MPa	7 Mpa
Elastic limit	30 Mpa	15-20 MPa Elongation at break 180%	? Elongation at break 140%
Max Von Mises constraints inside the glue (#thickness)	1 mm : 50 MPa 2 mm : 37 Mpa	⌀ 1 mm :13 MPa	1 mm : 0,31 MPa
	Hard epoxy does not fit	EP 37 stands the dilatation safety margin : 1,2	93500 stands the dilatation safety margin > 7



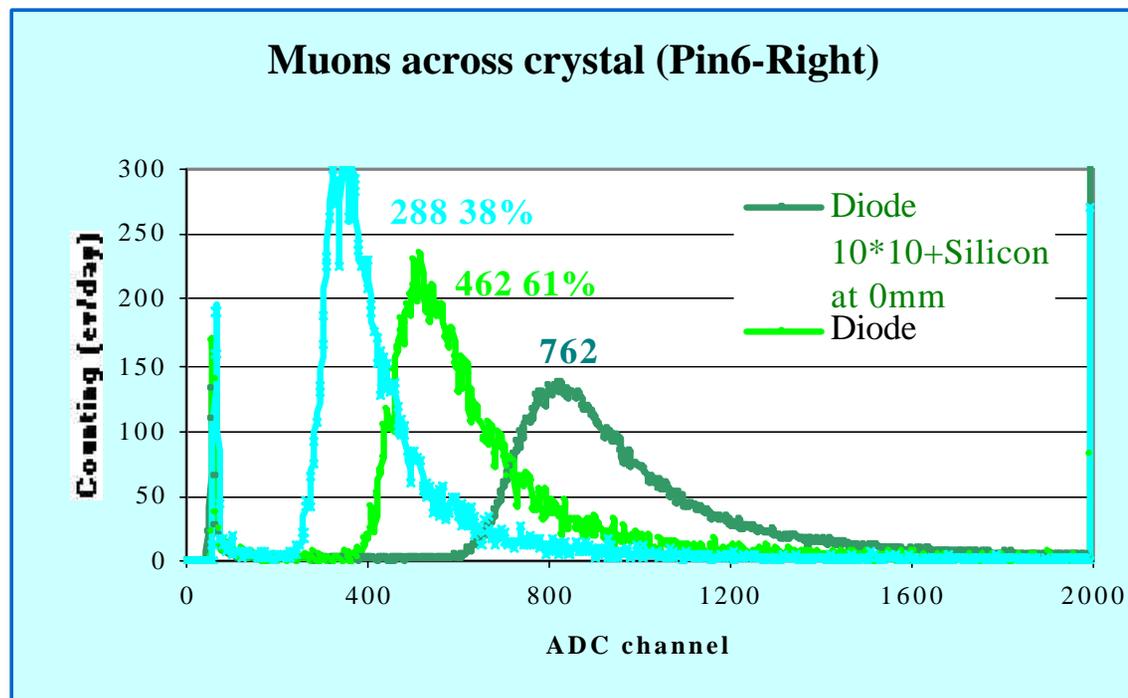
Bonding Plan

- Two soft glues would stand : soft epoxy & silicoïde with primer
- A vacuum gap is the back up solution.
- Thermal (-30°C to +50°C) cycling in vacuum environment tests between glass (same dilatation coefficient as diode) and Xtal Csl with surface preparation (roughness Ra between 3,2 and 6,4) is giving good coupling results.
- The type of bonding will be chosen after 12 thermal-vac cycles. A set of photodiodes that are larger than CAL DPD will be bonded on Csl and ultimately tested for 100 cycles.
- Aging tests (thermal cycling and irradiation) are performed on these glues having regard to transparencies results (cf irradiation tests)
- Bonding for FM and QM will follow the flow chart



Bonding Back up Solution

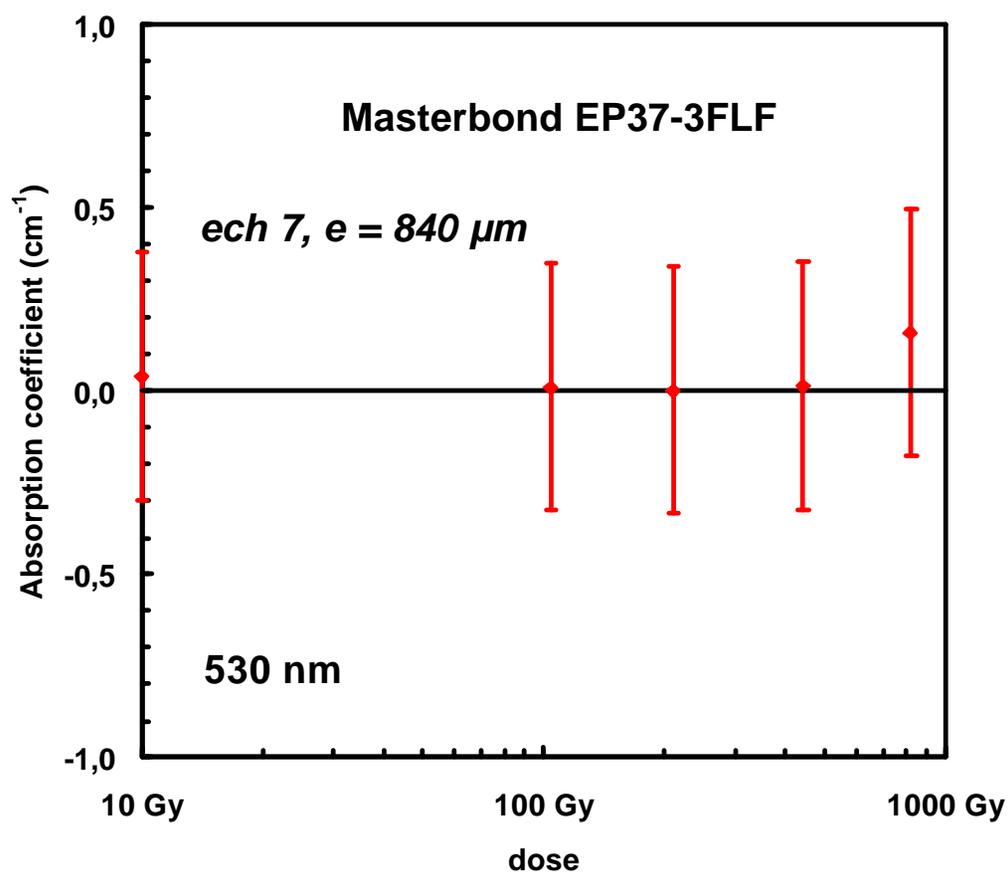
- ❑ Light yield vs. gluing, silicon pad, and air gap
- ❑ Backup = vacuum gap
 - impact on light yield ~ 50% lost

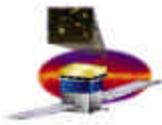




Absorption a_{induit} of EP37-3FLF vers. dose

- No significant effect has been seen on the wavelength band of the Emitted spectra of CsI(Tl).





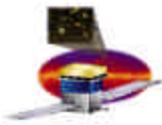
CDE tests

❑ Visual inspection

- press a prism with silicon on the side of the crystal in order to check the lack of bubbles
- check the lack of overflowing of bonding.

❑ Optical test

- The CDE test bench uses collimated gamma-rays from a radioactive source to test on the CDE properties. A XY table is used to place the source on 16 measurement points(TBR).
- if we can get a ^{228}Th radioactive source the 2.6 MeV signal will be used to test both small and big PINs.
- If we only are able to get a ^{22}Na (1.275 MeV line)
 - The XY table will help to test CDE properties (big PIN Diode)
 - The UV laser beam is only used for monitoring the small PIN signal during the set-up of the bench, relative to that of the big PIN obtained by a ^{22}Na 1.275 MeV line.



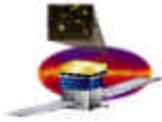
CDE facilities and Milestones

❑ Facilities

- A humidity plan is foreseen at every point of test and assembly and at every transportation.
- Clean room will be the area of assembly and test CDE

❑ Milestones

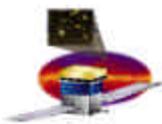
- VM2 : last CDE ready on 27 september 2001
- EM : last CDE ready on 21 December 2001
- FM-A last CDE ready on 14 November 2002
- FM-B last CDE ready on 12 December 2002
- Rate of 96 accepted CDE for the 16 FM must be of 20 days to be able to serve the last FM16 on time.



PEM Integration and Test

Gilles Bogaert
LHNPE Ecole Polytechnique

With Oscar Ferreira : assembly + environmental tests
Pierre Prat: System Engineer
Alain Debraine: Electronic Engineer
Veritas: Quality

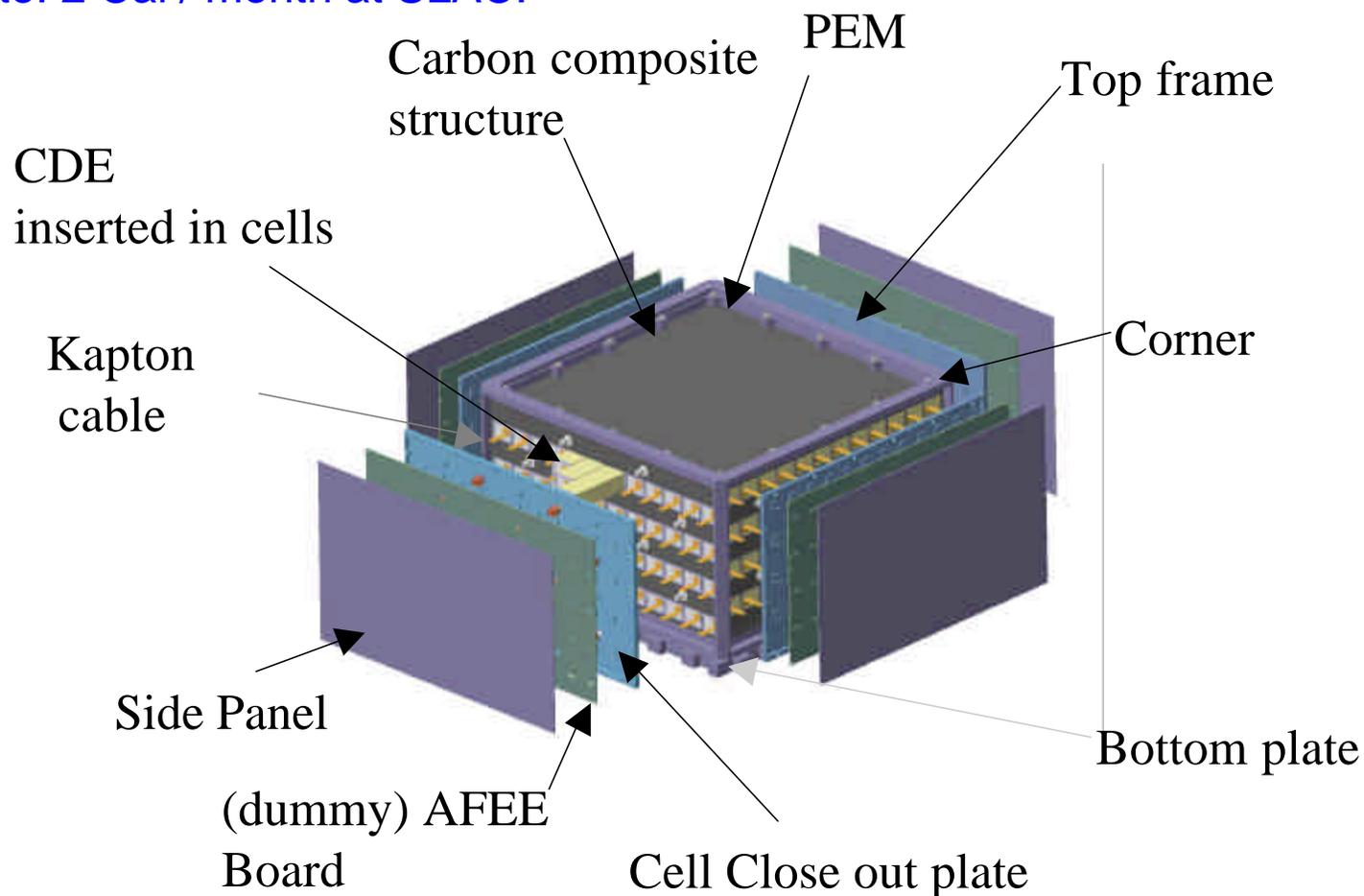


Calorimeter Tower Assembly

PEM Structures : EM(1+1) +18 Flight

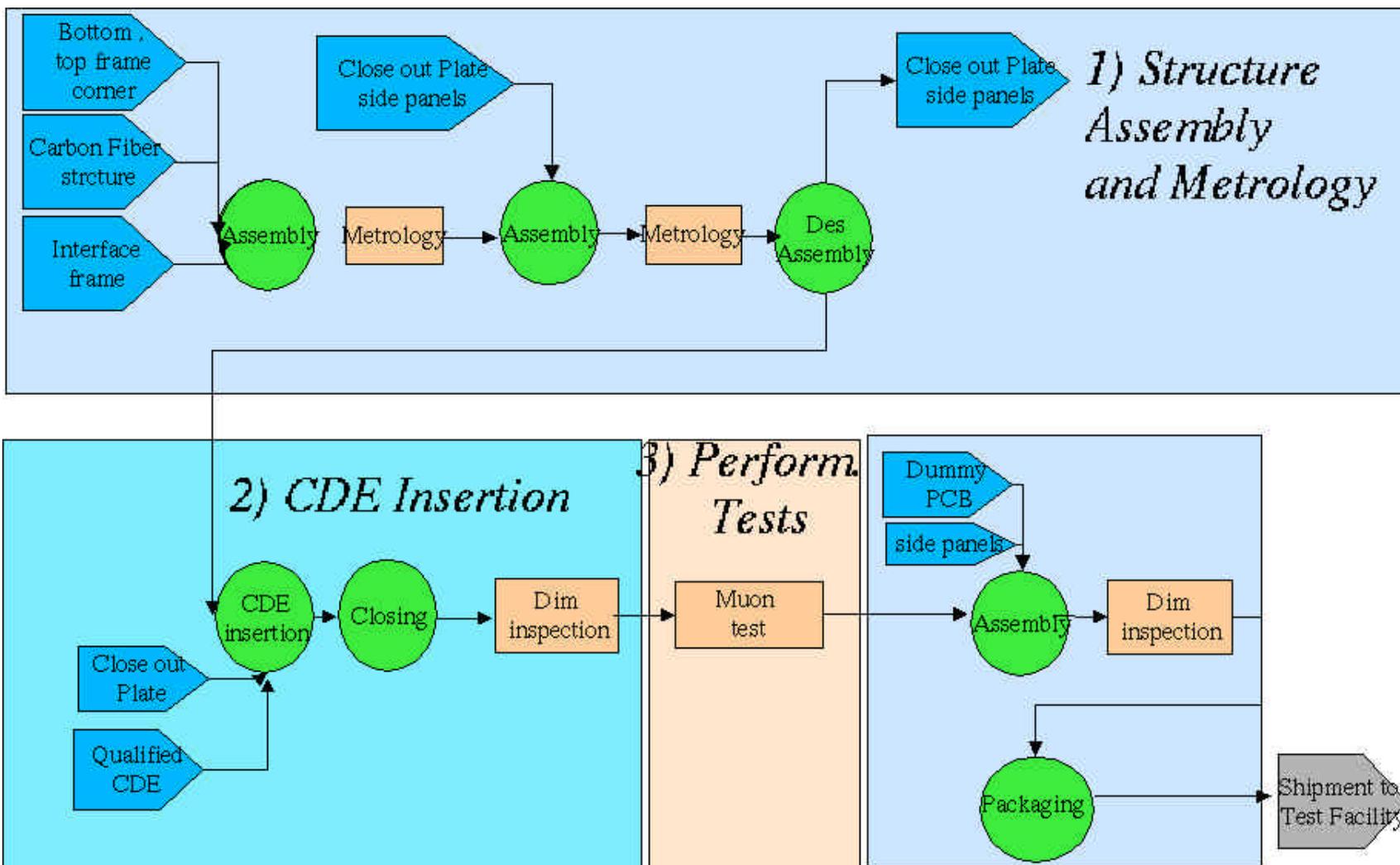
CDE: 96 in each CAL : 1824 CDE's + spares

Delivery rate: 2 Cal / month at SLAC.



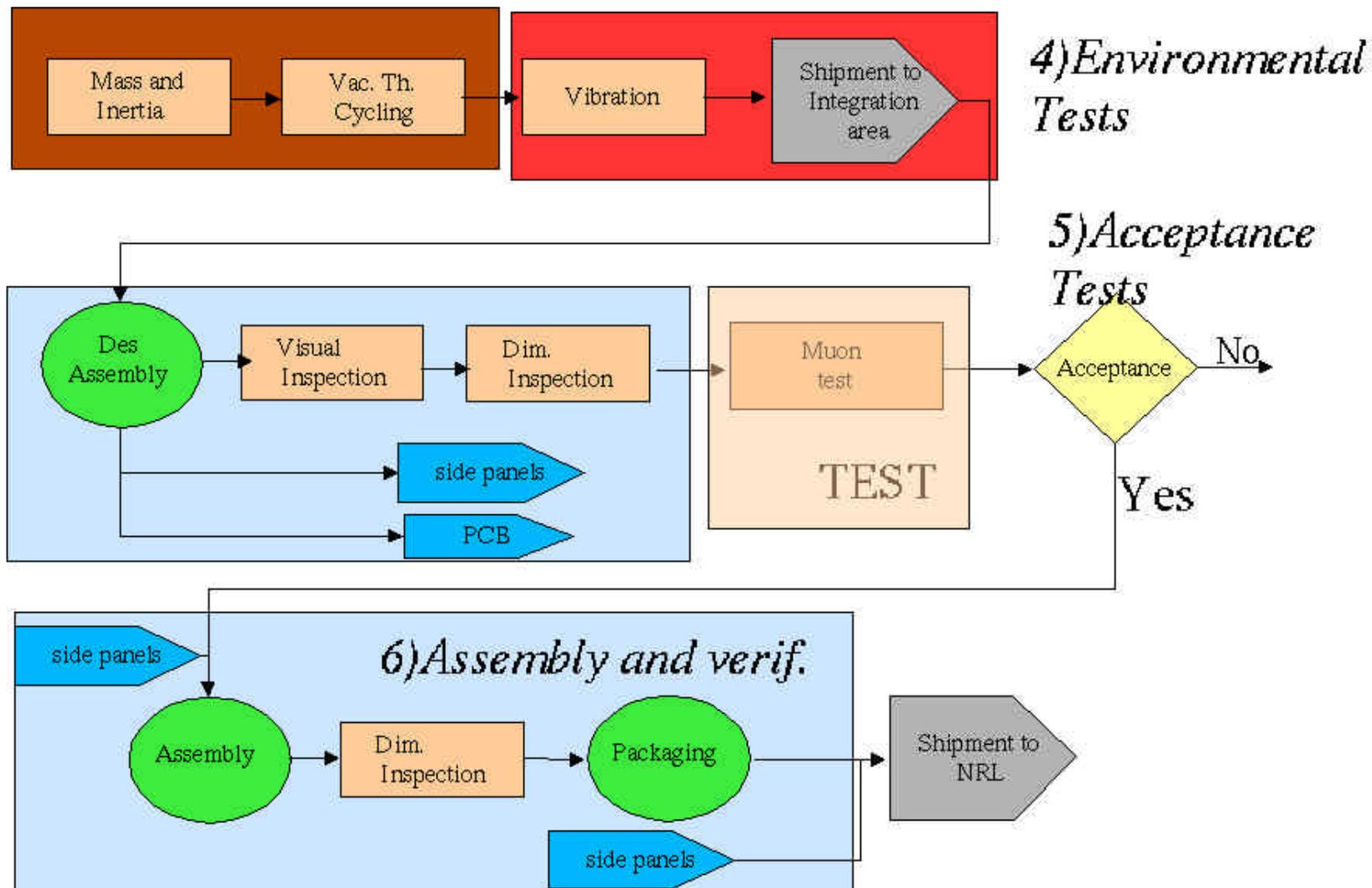


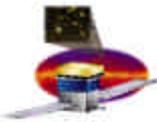
Assembly and Test Flow (1)



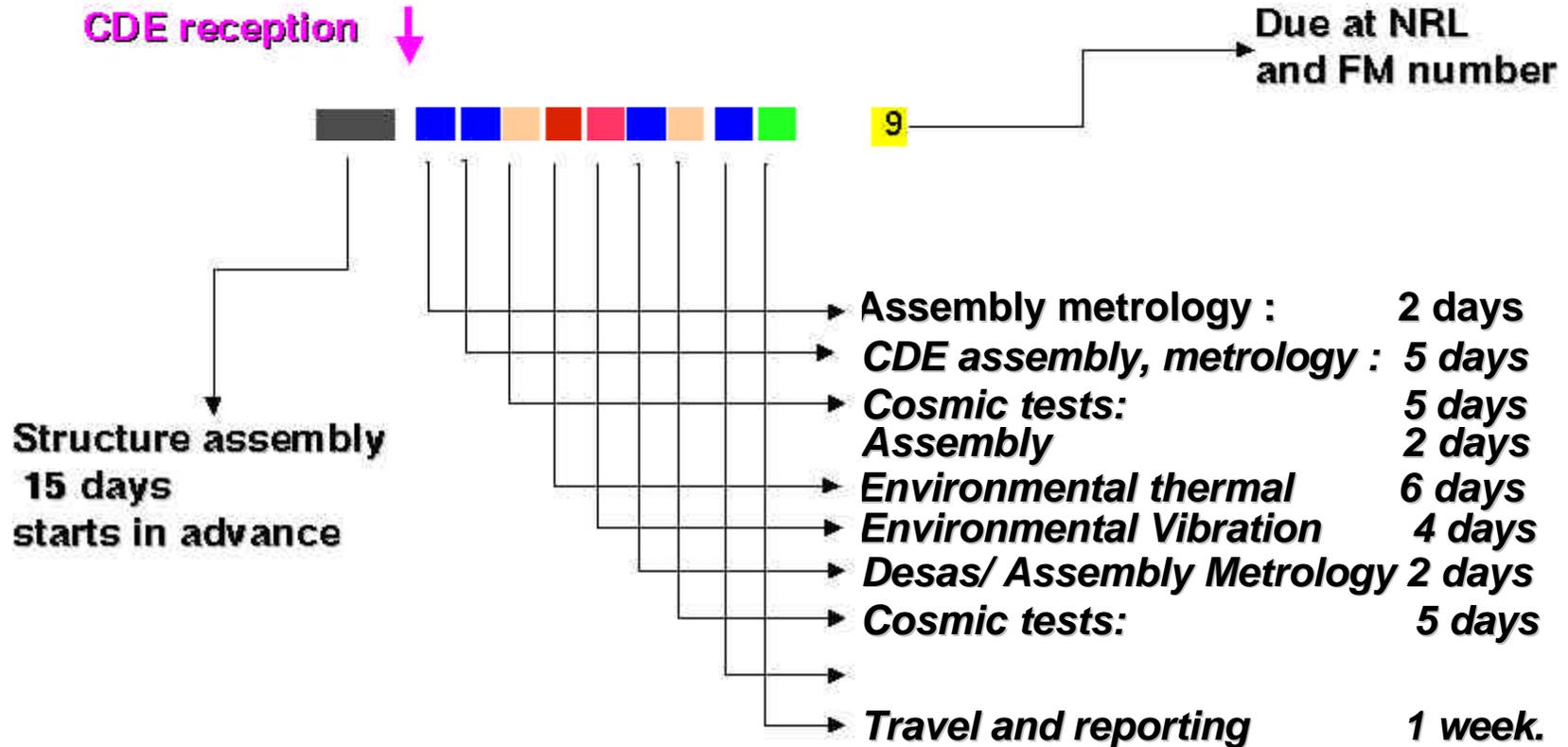


Assembly and Test Flow (2)

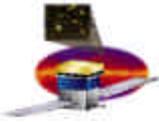




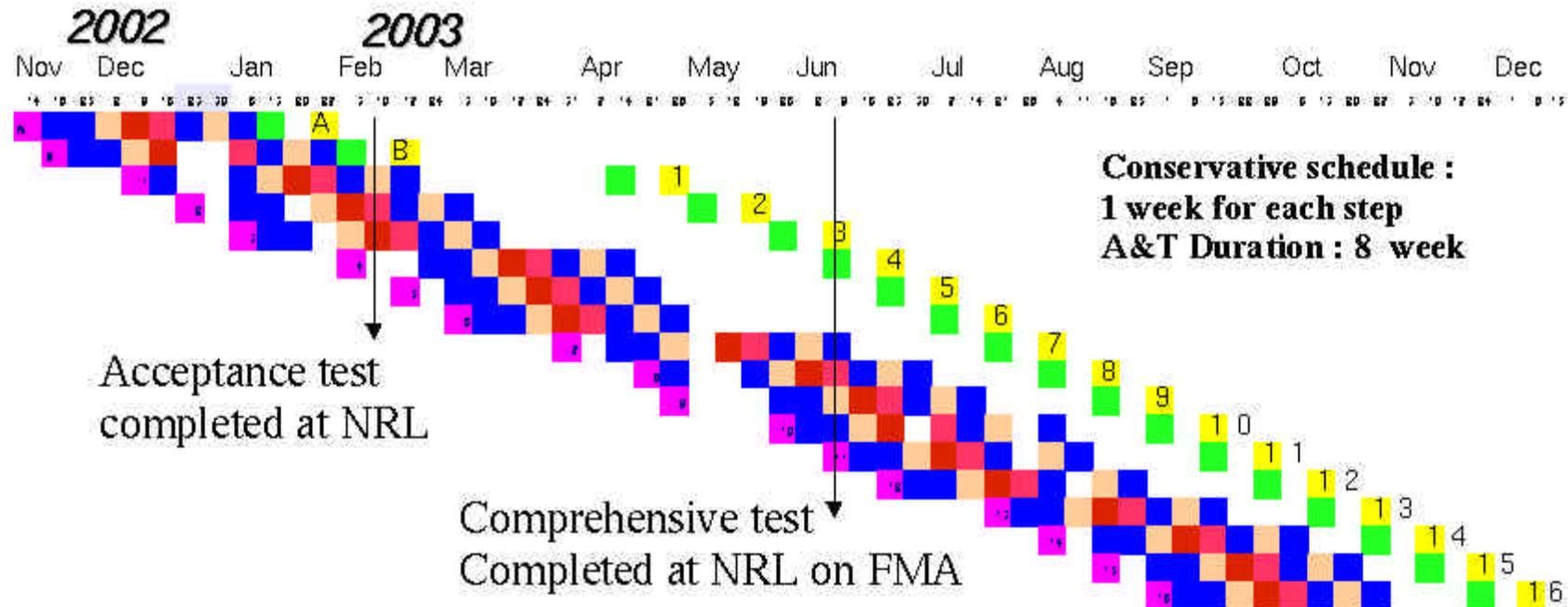
Assembly and Test Schedule (1)



Total duration from Assembly start to NRL: 7 weeks + 1 week travel to NRL



A&T Schedule Conservative



- ❑ Summer holidays and days off are drivers for FM 10 to 16.
- ❑ Last FM delivered 4 weeks before date.
- ❑ 3 to 5 PEM's in the flow at a time reporting included.
- ❑ Some margin left for holdups in this conservative schedule.
- ❑ Concern: Environmental facilities must be available nearly full time.
- ❑ Concern: FM 1 to FM 9 assembly starts before FMA fully tested at NRL.



Assembly Facility

□ Clean rooms (Polytechnique, P. Poilleux)

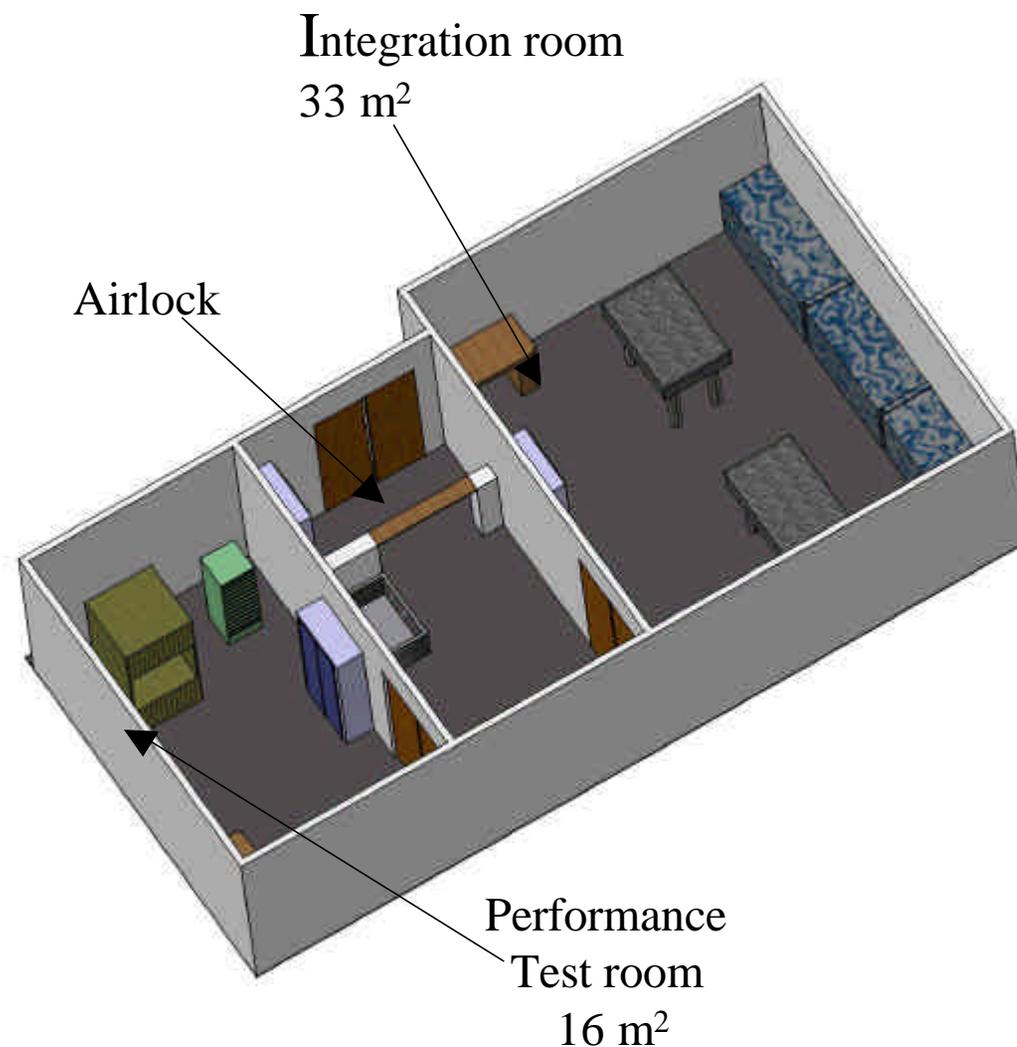
- Iso 7 (~ class 100 000)
- Temperature regulated 19 - 23°C
- Humidity regulated (40% HR)
- Construction started.
- Ready end 2001

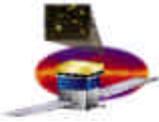
□ Integration room

- Allows storage of parts,
 - structures, CDE's
- 2 assembly plans :
 - CDE integration +
 - preintegration and closing

□ Air lock

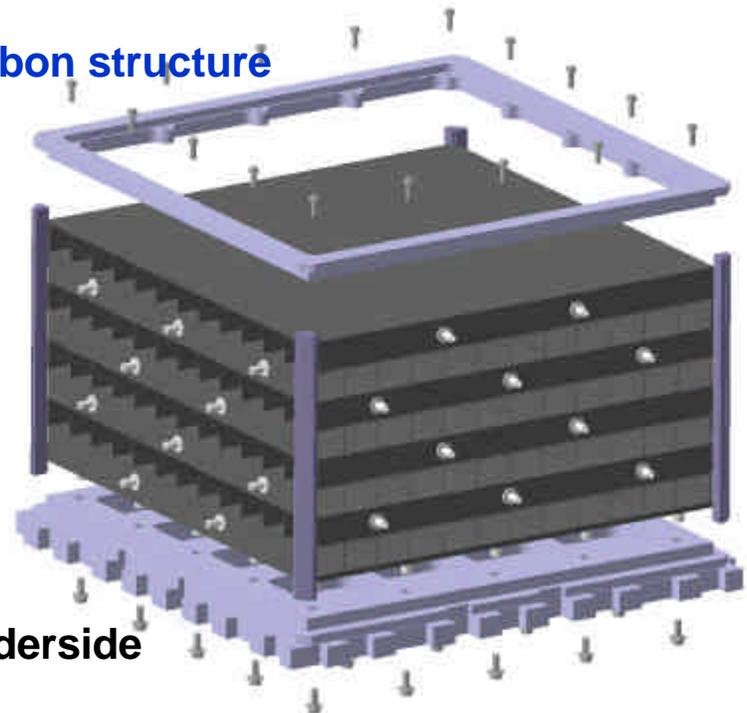
□ Test room: Cosmic EGSE





Structure Integration

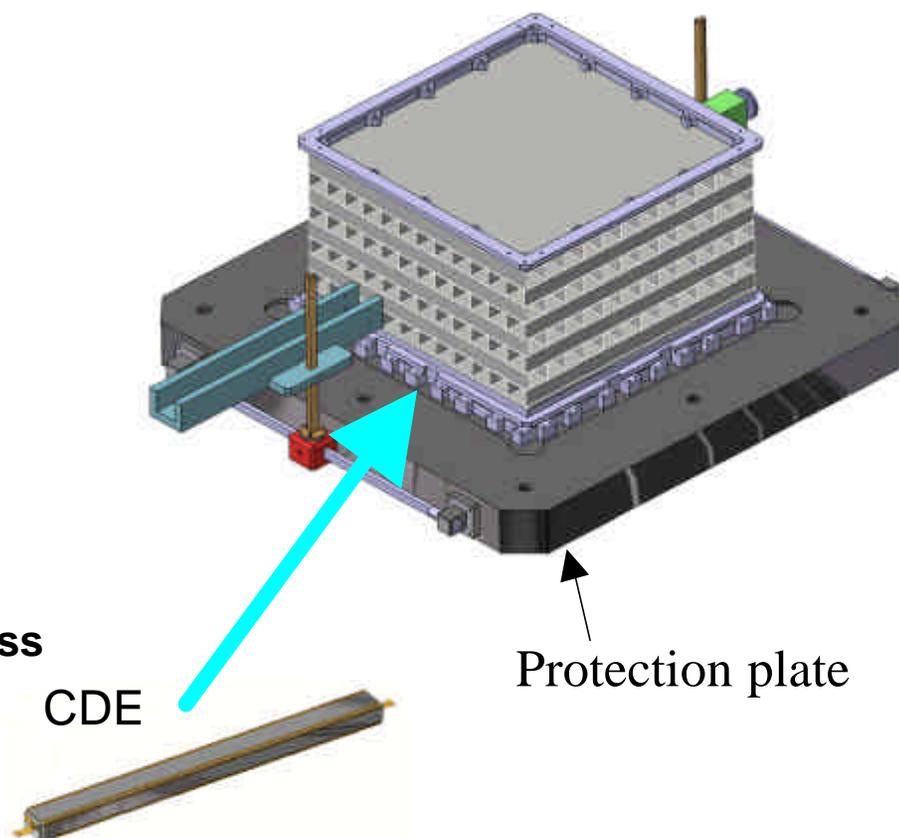
- ❑ Reception of mechanical part: in sealed bags;
 - storage in Assembly Room
 - all part are clean and inventoried
 - reception of CDE : storage inside cabinets with HR 5%.
- ❑ Structure assembly :
 - Attachment of Frames + Corners, to Carbon structure
 - Frame and Bottom plate have orientation marks
 - alignment controled,
 - screws tightened with torque
 - heads coated with a point of medium strength glue
- ❑ Mounting of Close Out plate
 - and Side Panel for metrology purpose
- ❑ Dismounting ... Ready for CDE integration
- ❑ Protection plate fixed at the Bottom Plate underside
 - through dedicated holes.
 - also used for environmental tests)





CDE Integration

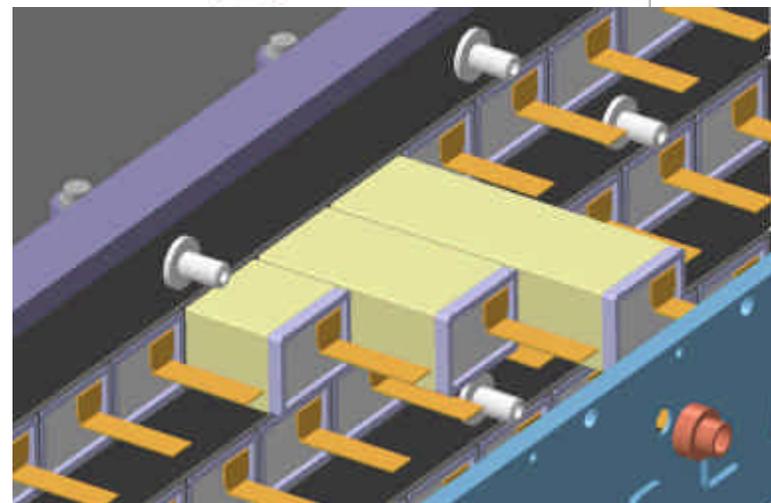
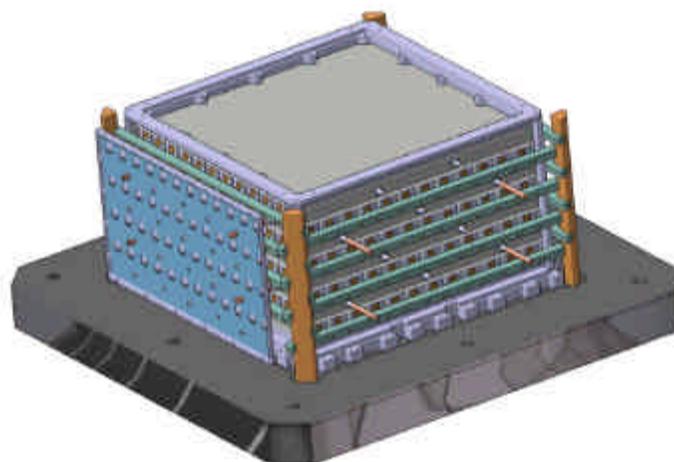
- ❑ Tooling for CDE integration into the Structure cell
 - Precise alignment of CDE with Structure cell
 - attachment of stretched elastomeric cords
 - provide a stop for the log at accurate position
- ❑ A jig is used for positioning the U shape part
- ❑ CDE are removed from support blocks, and placed in the U shape part.
 - A protection is used during insertion for Kapton cable.
- ❑ Damper Frames of desired thickness put in place at log ends
- ❑ Elastomeric cords released





Assembling Close Out Plates

- ❑ Flex cables (brown in the figure) kept horizontally using a tool
- ❑ Flex inserted in Close Out plate
- ❑ Tool removed
- ❑ Close Out plate in contact with structure
- ❑ Close Out plate positioning and screw tightened with a torque
- ❑ Point of medium strength glue at defined position on screw head
- ❑ Attachment of interface blocks at top frame corners for structure lifting.
- ❑ Ready for transfer to test room using transportation cart.





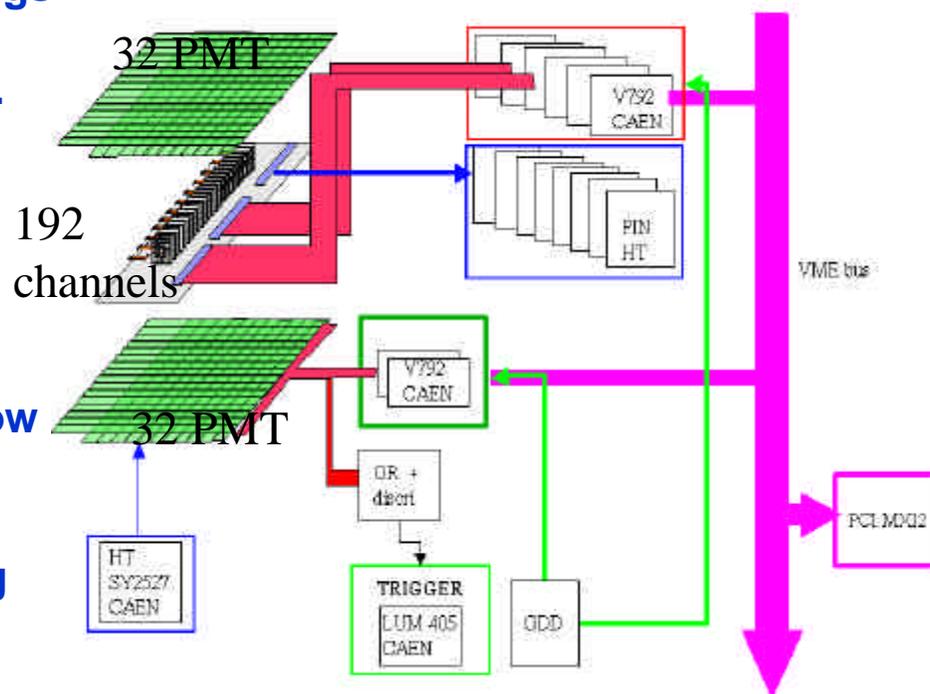
Optical Test Using Cosmic Muons

- ❑ **Performance tests**
 - Check the CDE Light Yield performances with cosmic muons
- ❑ **Requirements:**
 - Light tapering monotonic in the range 0.4 to 0.75
 - Large diode: 5000 e/MeV- Small diode: 800 e/MeV
 - Scattering of Light Yield performances, at < 15 % resolution
- ❑ **EGSE : Cosmic muon test bench**
 - Muon hodoscope
 - Electronic and data acquisition system for 192 channels.
 - Localized in clean room.
 - Output : light Yield and attenuation maps
 - Spares for electronics and telescope.
- ❑ **Test Duration**
 - EM: 5 weeks
 - FM: 1 week



Cosmic EGSE

- ❑ Analog and digital system for 192 channels
 - at the same time (X logs or Y logs small and large diodes)
 - 2 sets of measurement needed.
- ❑ Absolute light yield calibration:
 - Gain calibration using ^{241}Am Source or charge injection.
- ❑ Signal processing
 - same as AFEE ASIC
 - Hybrid Preamp + shaper with low noise close to PIN diodes.
 - Charge ADC's
 - Discriminator for self triggering (Calibration)
- ❑ Muon Hodoscope
 - Tapering and position resolution.
 - Provides the Trigger signal





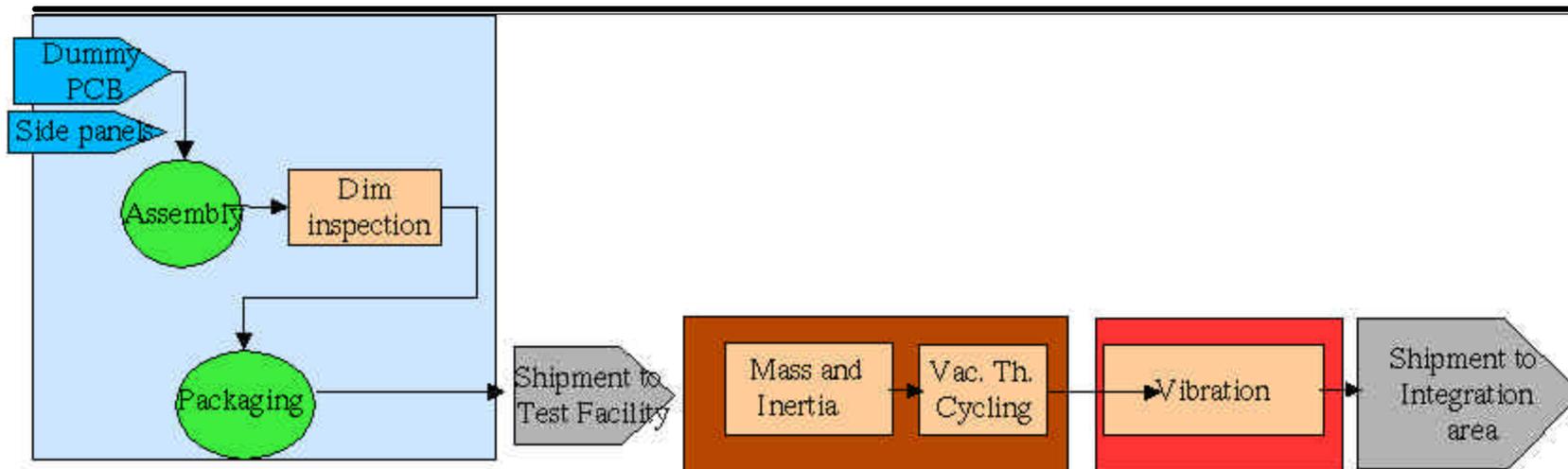
Environmental Test

	TESTS	VM2	EM-PEM	QM-PEM	FM-PEM	FSM-PEM
STRUCTURAL & MECHANICAL	MODAL SURVEY	M	M	M	M	M
	STATIC LOADS	M	M _(TBC)	N.A.	N.A.	N.A.
	ACCELERATION	N.A.	N.A.	N.A.	N.A.	N.A.
	SINE BURST	Q	Q	Q	A	A
	SINE VIBRATION (TBC)	Q	Q	Q	A	A
	RANDOM VIBRATION	Q	Q	Q	A	A
	ACOUSTICS	N.A.	N.A.	N.A.	N.A.	N.A.
	MECHANICAL SHOCK	N.A.	N.A.	N.A.	N.A.	N.A.
	PRESSURE PROFILE	Q	Q	Q	A	A
	TORQUE RATIO	N.A.	N.A.	N.A.	N.A.	N.A.
	LIFE TESTS	N.A.	N.A.	N.A.	N.A.	N.A.
	MASS PROPERTIES	M	M	M	M	M
	THERMAL	LEAK	N.A.	N.A.	N.A.	N.A.
	THERMAL-VACUUM CYCLE	Q8	Q4	Q2	A1	A1
	THERMAL CYCLES (NON VACUUM)	N.A.	N.A.	N.A.	N.A.	N.A.
	THERMAL BALANCE	M	N.A.	N.A.	N.A.	N.A.
	TEMPERATURE-HUMIDITY	N.A.	N.A.	N.A.	N.A.	N.A.
	BAKEOUT	N.A.	N.A.	N.A.	N.A.	N.A.
	PERFORMANCE TEST @ TEM	N.A.	N.A.	N.A.	N.A.	N.A.

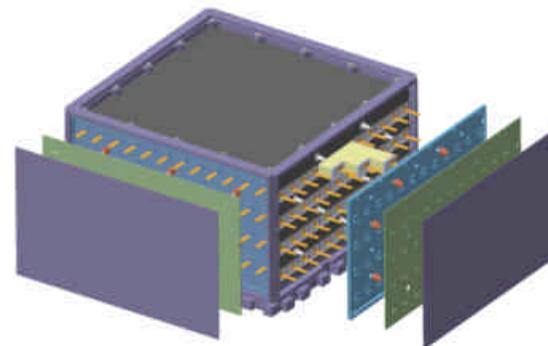
VM2 and Qual Model tested at qualification levels

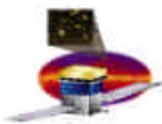


Environmental Testing

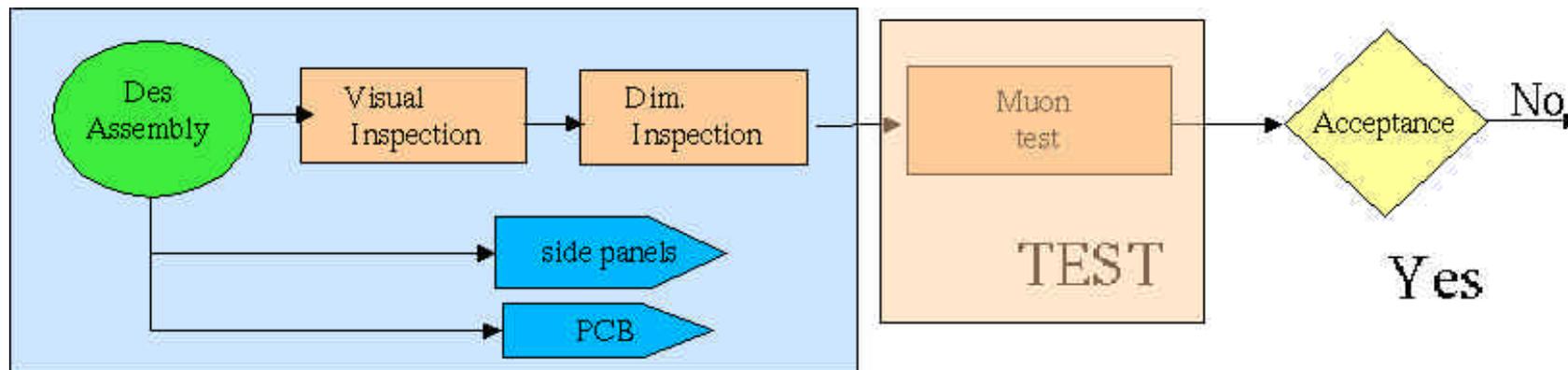


- Dummy AFEE instrumented
 - Inserted on each PEM side
- Flex inserted in connectors
- Placed in container
- Shipped to facility
 - (Intespace Toulouse TBR)
- On engineer at Facility for reception, instrumentation

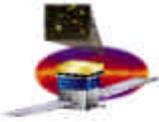




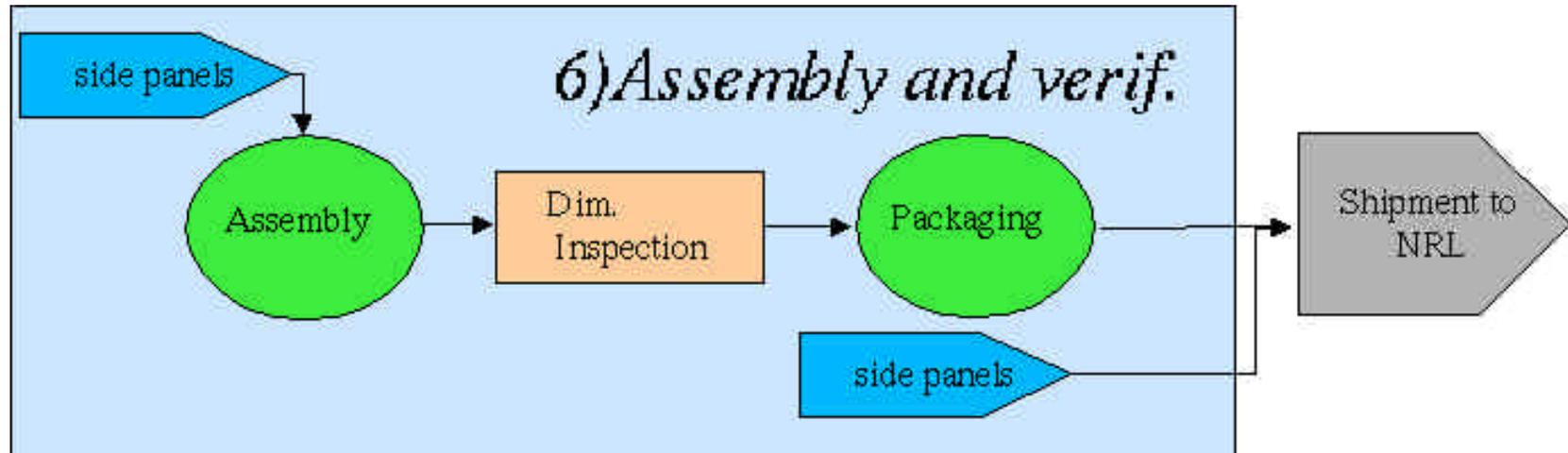
Post Environmental Testing



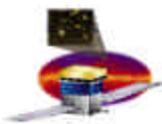
- ❑ Dummy AFEE instrumented removed
- ❑ Metrology
- ❑ Second muon test
- ❑ Comparison of results with first muon test ones is final acceptance test.



Final Inspection and Shipment

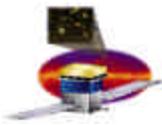


- new protection plate protects the Bottom Plate underside
- Kapton cables are attached for transportation
- Shipment box is still TBD.
- New screws are sent together with Side Panels.



PEM Assembly & Test: Resource Allocation

- ❑ **Clean room:**
 - 1 engineer (P. Poilleux) from Mech. Engineering Group
 - new organization of Mech. equipment. Clean room building : specification written, orders started July 2001.
 - Quality and organization : 1 month of specialist planned to initiate working in clean room (during EM assembly).
- ❑ **VM2, EM and FM Assembly: Mech. Engineering Group + 1**
- ❑ **Environmental Test : 0.5 engineer at Facility**
- ❑ **Cosmic EGSE: in development. OK**
- ❑ **Resources and management experience in same kind of organization structure (Aleph, LEP, ...)**
- ❑ **Additional resources: exist in the Mech Engineering Group to face human problems (broken legs ...) and technical breakdown. Possibility of resorting to qualified additional manpower for delivering flow achievement**
- ❑ **Quality insurance: provided by Veritas**

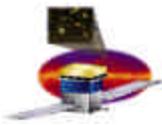


Conclusions, Issues and Concerns

- ❑ **Concerns :**
 - **Integration of FM B to FM 4 must be started before PEM FM A acceptance test completed at NRL.**

- ❑ **Possible concern: Acceptance test with cosmic muons at NRL**
 - **Instruments at NRL and Polytechnique should be intercalibrated ?**

- ❑ **TBR: Thermal Cycling Facility must be available for ~1 year.**

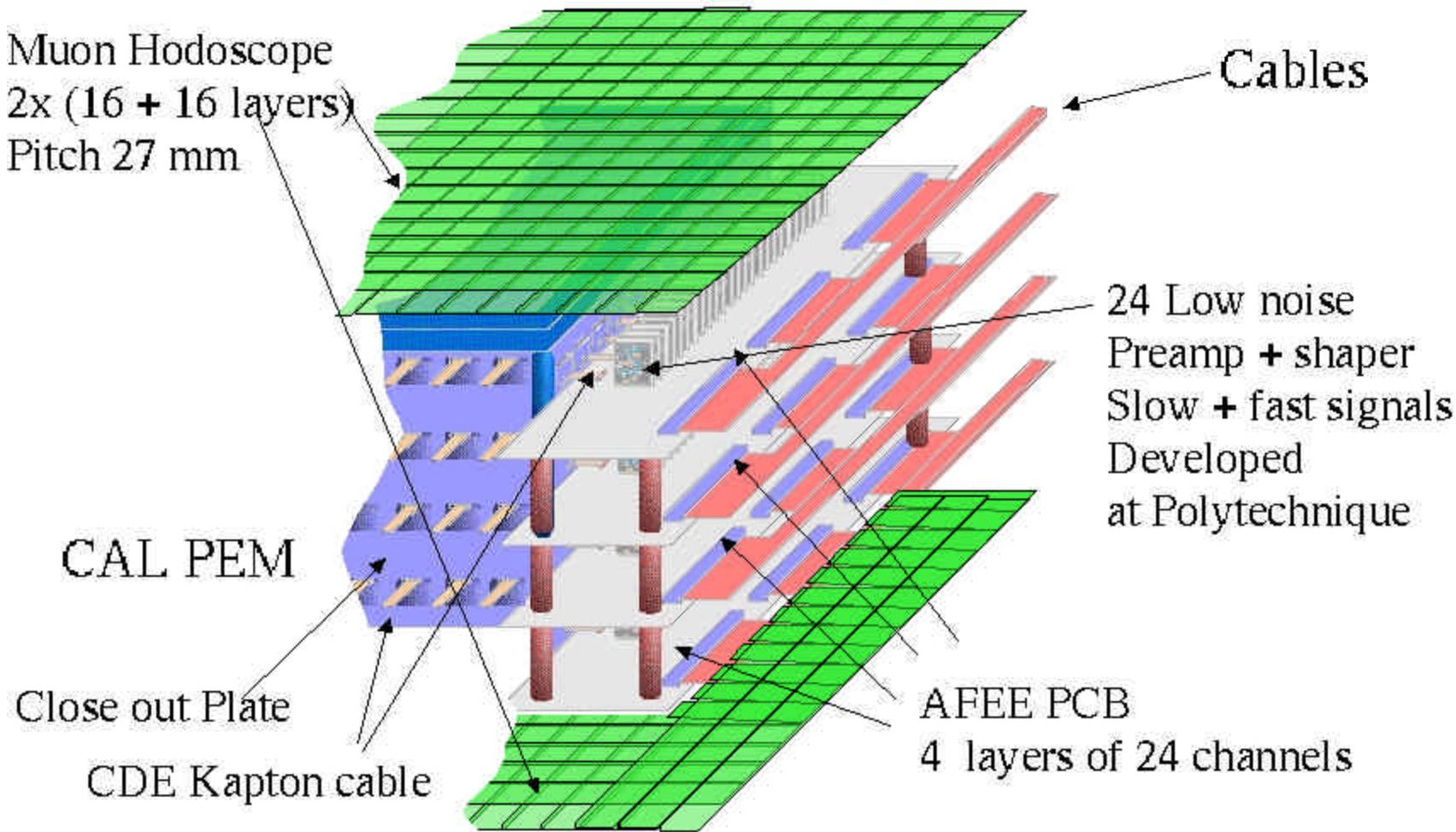


Cosmic EGSE (2)

- ❑ **Off shell electronics ordered and partially delivered.**
- ❑ **Custom electronics**
 - **20 Prototypes in test (A. Debraine).**
 - **mass AFEE hybrid circuits delivered in December**
 - **PCB, connectors, delivered in September**
- ❑ **New Hodoscope**
 - **subcontracted by Saclay SED. Delivery in September 2001**
- ❑ **Software based on labview**
 - **in development. Completed November 2001**
- ❑ **Mechanics: Fab starts in September Resp: M. Gladieux (CdF)**
- ❑ **Hardware**
 - **Assembled Dec 1/01**
 - **Ready 1/1/2002.**



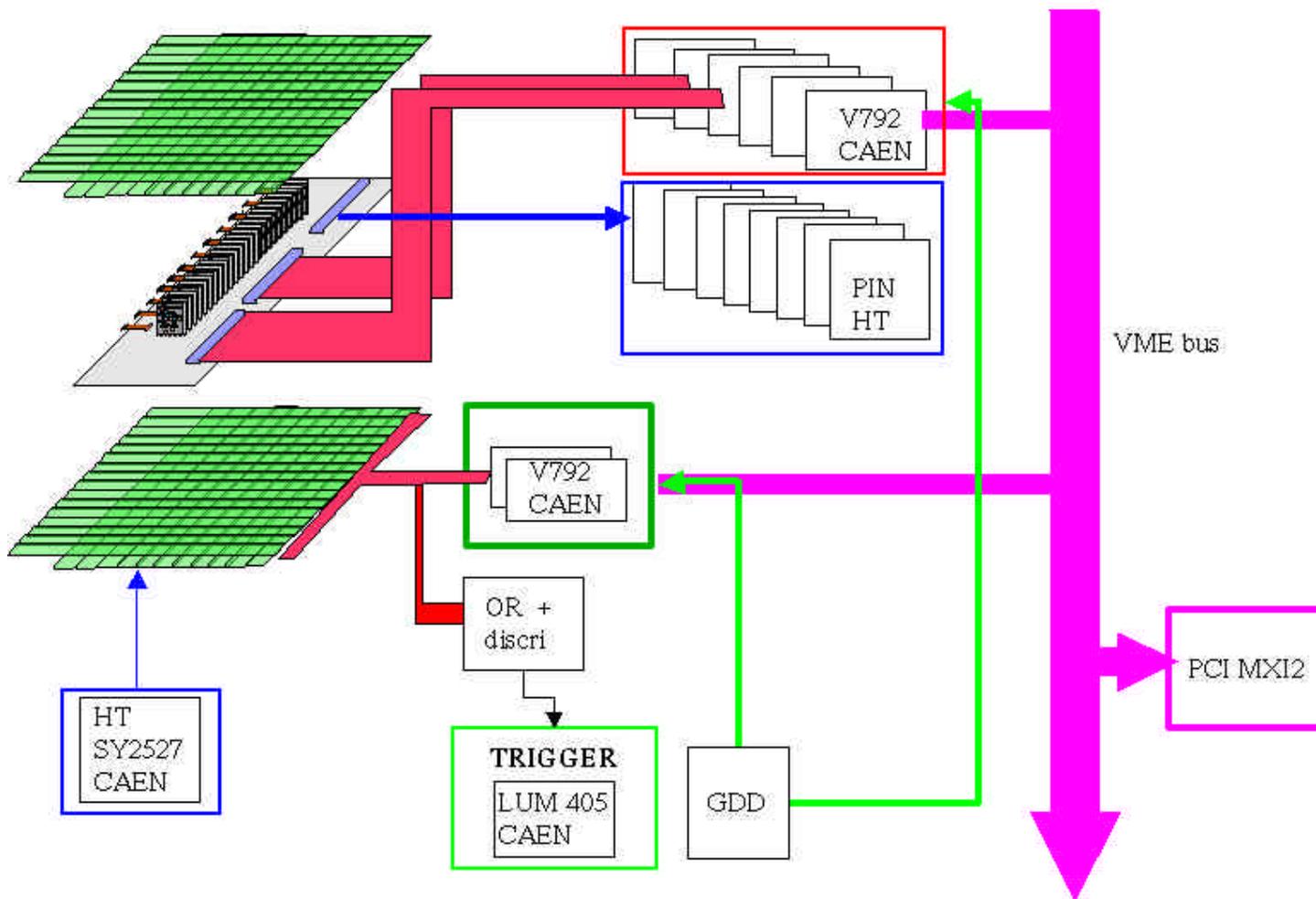
Cosmic EGSE Design

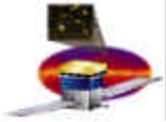


+ Shielding box and cooling



Cosmic EGSE Electronics





Electronics Design

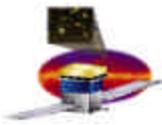
James Ampe
NRL / Praxis, Inc.



Level IV Requirements

□ Energy Measurement Dynamic Range

- Log end electronics shall process energy depositions in the 2 MeV to 100 GeV range
- The low energy charge amplifier shall process energy depositions in the 2 MeV to 1.6 GeV range
 - The light yield measured by the large PIN photodiode shall be 5000 e⁻/MeV for energy depositions at the center of the CsI crystal
 - The equivalent noise (RMS) on the low energy slow shaped signal paths shall be less than 2000 e⁻, for maximum diode capacitance 90 pF
- The high energy charge amplifier shall process energy depositions in the 100 MeV to 100 GeV range
 - The light yield measured by the small PIN photodiode shall be 800 e⁻/MeV for energy depositions at the center of the CsI crystal
 - The equivalent noise (RMS) on the high energy slow shaped signal paths shall be less than 2000 e⁻ for maximum diode capacitance 25 pF



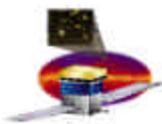
Requirements (2)

❑ Dead Time and Overload

- The dead time associated with the capture and measurement of the energy depositions shall be less than 100 μsec . The goal is less than 20 μsec .
- The calorimeter electronics shall be capable of recovery from a x1000 overload within 100 μsec . Recovery is defined as below the measurement readout (zero suppression) threshold.

❑ Cal Triggers

- The calorimeter shall provide a prompt (within 2 μs of an event) low-energy trigger signal to the LAT trigger system with a detection efficiency of greater than 90% (TBR) for 1 GeV gamma rays entering the calorimeter from the LAT field of view with a trajectory which traverses at least 6 Radiation Lengths of CsI.
- The calorimeter shall provide a prompt (within 2 μs of an event) high-energy trigger signal with a detection efficiency of greater than 90% for 20 GeV gamma rays entering the calorimeter from the LAT field of view that deposit at least 10 GeV in the CsI of the calorimeter.



Requirements (3)

❑ Power

- The conditioned power consumption of each calorimeter module shall not exceed 5.6875 W

❑ Circuit geometry

- Each calorimeter module shall include analog and digital readout electronics (AFEE) on the four vertical faces at the ends of the CsI crystal array

❑ Temperature

- The performance of the qualification electronics shall be tested over the qualification temperature range of -30 to 50 degrees C.
- The performance specifications of flight units shall be achieved over the operational temperature range of -10 to 35 degrees C

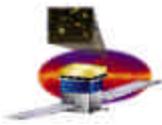
❑ Radiation Susceptibility

- The electronics shall be insensitive to Single Event Upset for LETs < 8 MeV/(mg/cm²).
- The electronics shall meet its performance specifications after a total radiation dose of 10 krad (includes margins)
- Calorimeter electronics latchup requirement: LET > 60 (MeVcm²)/mg



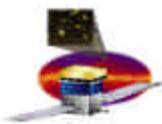
Derived Front-End Requirements

- ❑ The low energy fast shaped signals shall peak at $3.5 \pm 0.5 \mu\text{sec}$. All ASICs shall have the same peaking time $\pm 0.2 \mu\text{sec}$.
- ❑ The gain of both the low and high energy channels shall be adjustable by at least a factor of 2 in approximately 10 – 25% steps.
- ❑ Both the low and high energy fast shaped signals for triggering shall peak at $0.5 \pm 0.2 \mu\text{sec}$.
- ❑ The low energy fast shaping amplifier shall support the lowest ~25% of low energy range, i.e. nominally 400 MeV maximum energy.
- ❑ The high energy fast shaping amplifier shall support the entire low energy range, i.e. nominally 100 GeV maximum energy.
- ❑ The maximal non-linearity in each of the 4 ranges shall be 1 % of full range



Electronics Development

- **Design documentation for building the electronics:**
 - **Calorimeter Subsystem Design**
 - Calorimeter Subsystem Specification, LAT-SS-00018
 - Conceptual Design of the Calorimeter Electronics System , LAT-SS-00087
 - Calorimeter Grounding and Shielding Plan, LAT-SS-00272
 - **Special Component Design, Application Specific Integrated Circuits**
 - Conceptual Design of the Glast Calorimeter Front End Electronics ASIC, LAT-SS-00088
 - Glast Calorimeter Front End Electronics ASIC Specification, LAT-SS-00089
 - Conceptual Design of the Glast Calorimeter Readout Control ASIC, LAT-SS-00208
 - **Other special components**
 - Specification for the Calorimeter Photodiode Flexible Cable, LAT-SS-00211



Electronics Development (2)

□ Implementation of Design

– Mechanical Circuit Board Fittings

- Form fit and allocated space makes design a challenge

– Progress to Date

- Custom electronics (ASICS)
- Commercial/military electronic parts
- Tower electronics Module (TEM) electronics connection
- Power budget
- Grounding plan
- Interface definitions
- Parts List

– Issues to be resolved

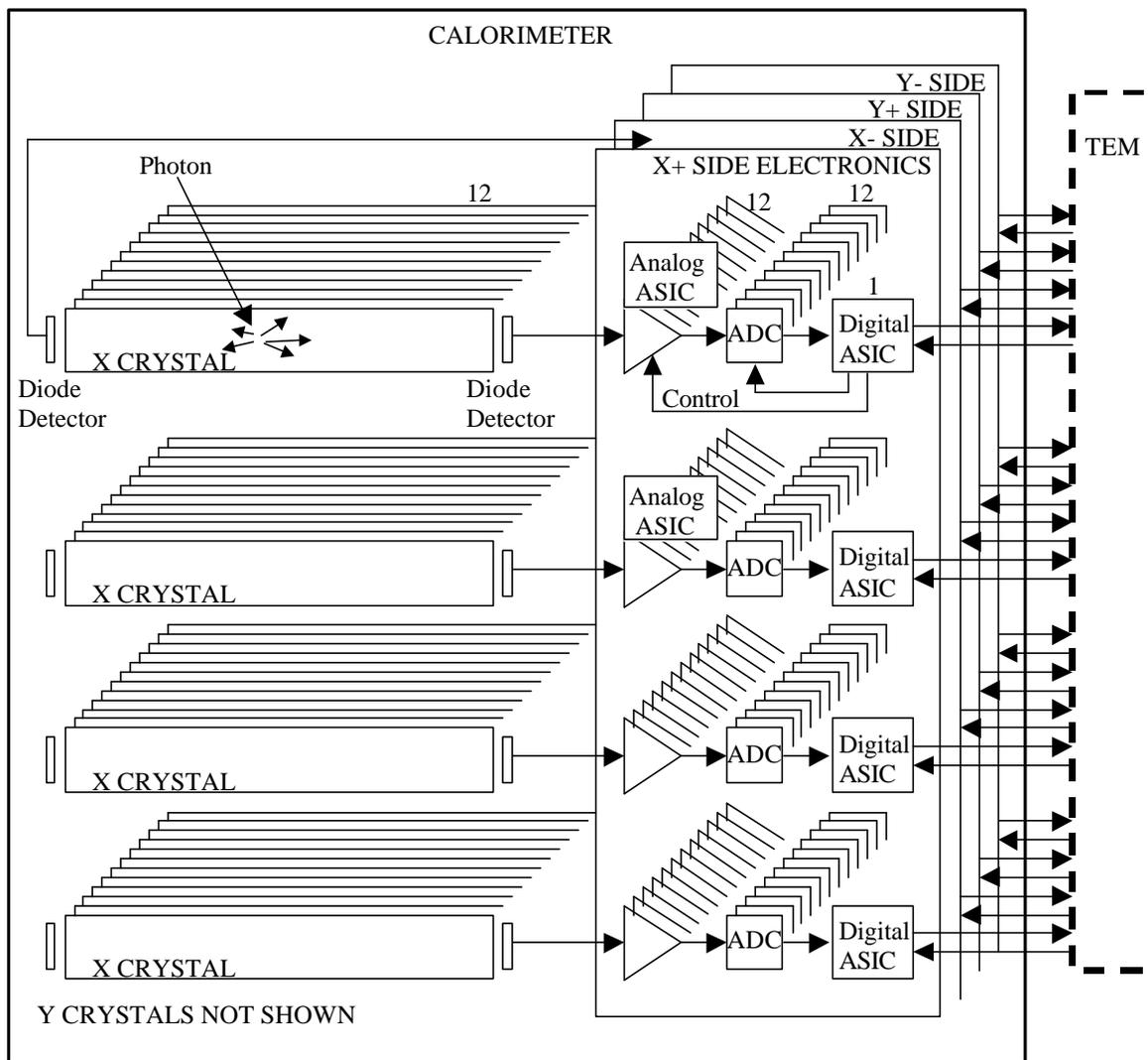
- Custom LVDS noise margins
- Assembled system front-end noise
- HP 0.5um designs latchup susceptibility



Functional Block Diagram

Redundancy in opposite log-end readout performed by different AFEE Board

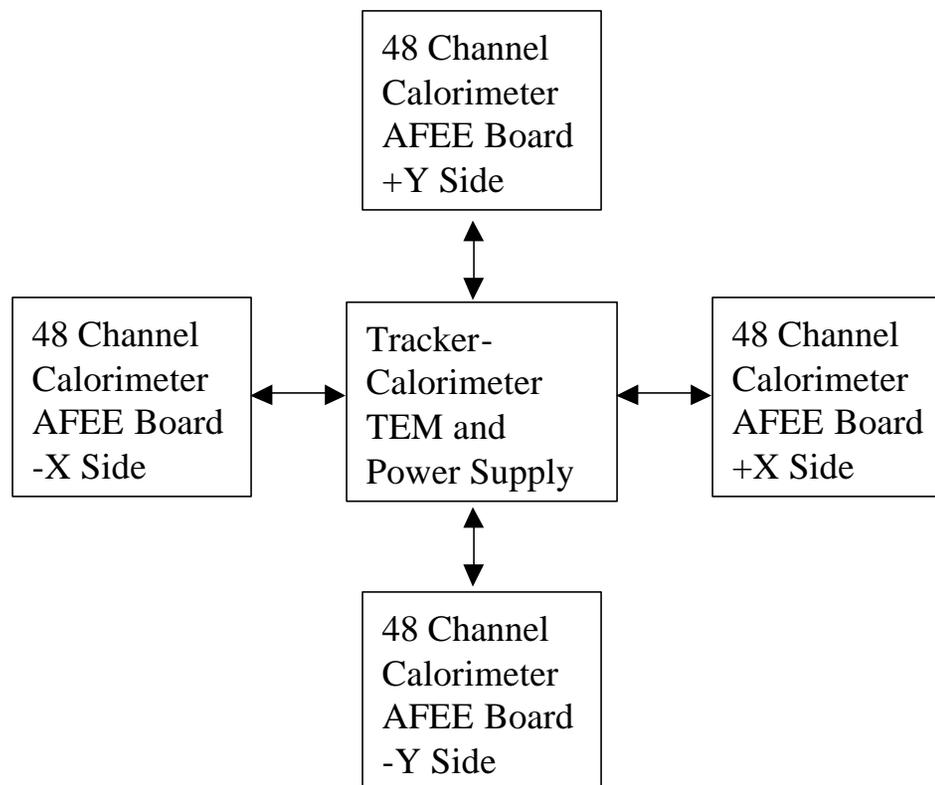
CALORIMETER FUNCTIONAL BLOCK DIAGRAM





CAL Electronics System

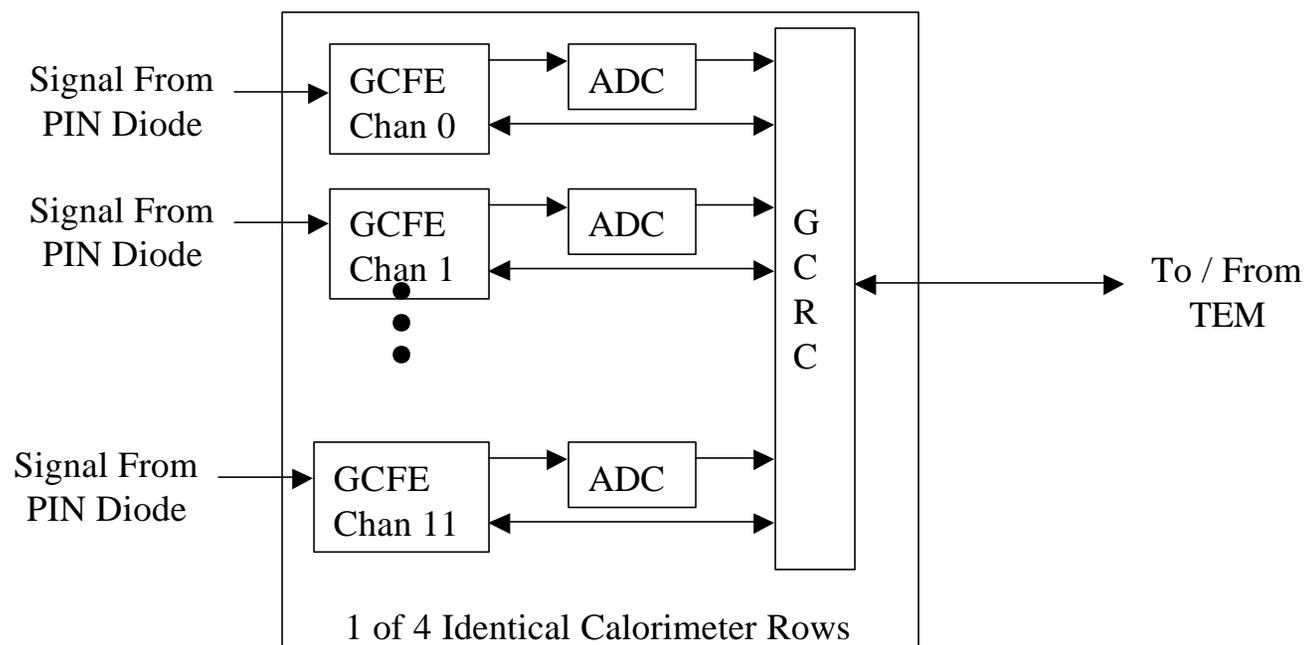
- ❑ Cal readout electronics physical constraints:
 - 1 Cal electronics board (AFEE) per calorimeter side.
 - Each Cal circuit board communicates to Tower Electronics Module (TEM) mounted below calorimeter
 - The TEM correlates crystal end readouts, zero-suppresses the AFEE data and formats the event message for the T&DF.
 - Redundant system, CAL can operate with loss of 1 X and 1 Y side

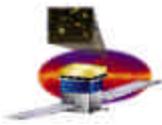




CAL AFEE Design

- Cal AFEE sideboard design, electronics grouped by rows
 - 1 analog ASIC (GCFE) and commercial ADC per log end
 - 1 Digital ASIC per row (GCRC), communicates between GCFE - ADC pair (12 pairs per row) and external TEM
 - Partitioned design - failure of 1 GCRC only removes 1 row. Would still meet mission requirements.





GCFC ASIC Features

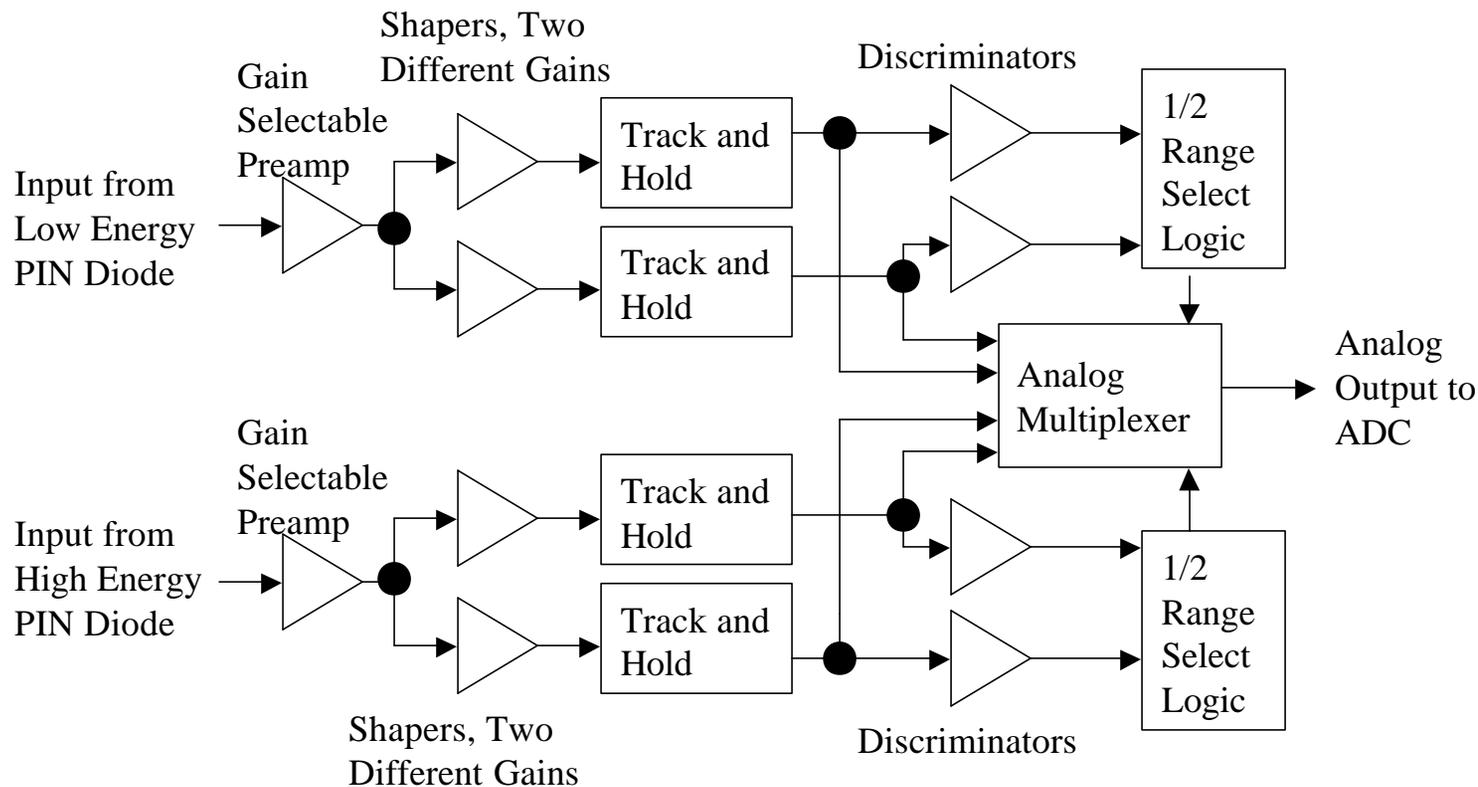
- ❑ GCFC design by SLAC using LAT-wide design concepts and features

- ❑ GCFC Analog Custom ASIC, main features
 - 1 GCFC per log end, each GCFC accepts two diode signal inputs
 - Each diode input has two amplifier signal paths
 - External resistors and capacitors used for shapers
 - 2 diode 2 amplifier combination results in 4 overlapping gain ranges, per log end.
 - Each GCFC individually addressable on a command bus
 - Command bus and digital control use Low Voltage Differential Signaling (LVDS) to minimize front-end injection
 - Target package, 44 pin 10 mm square body quad flat pack package.



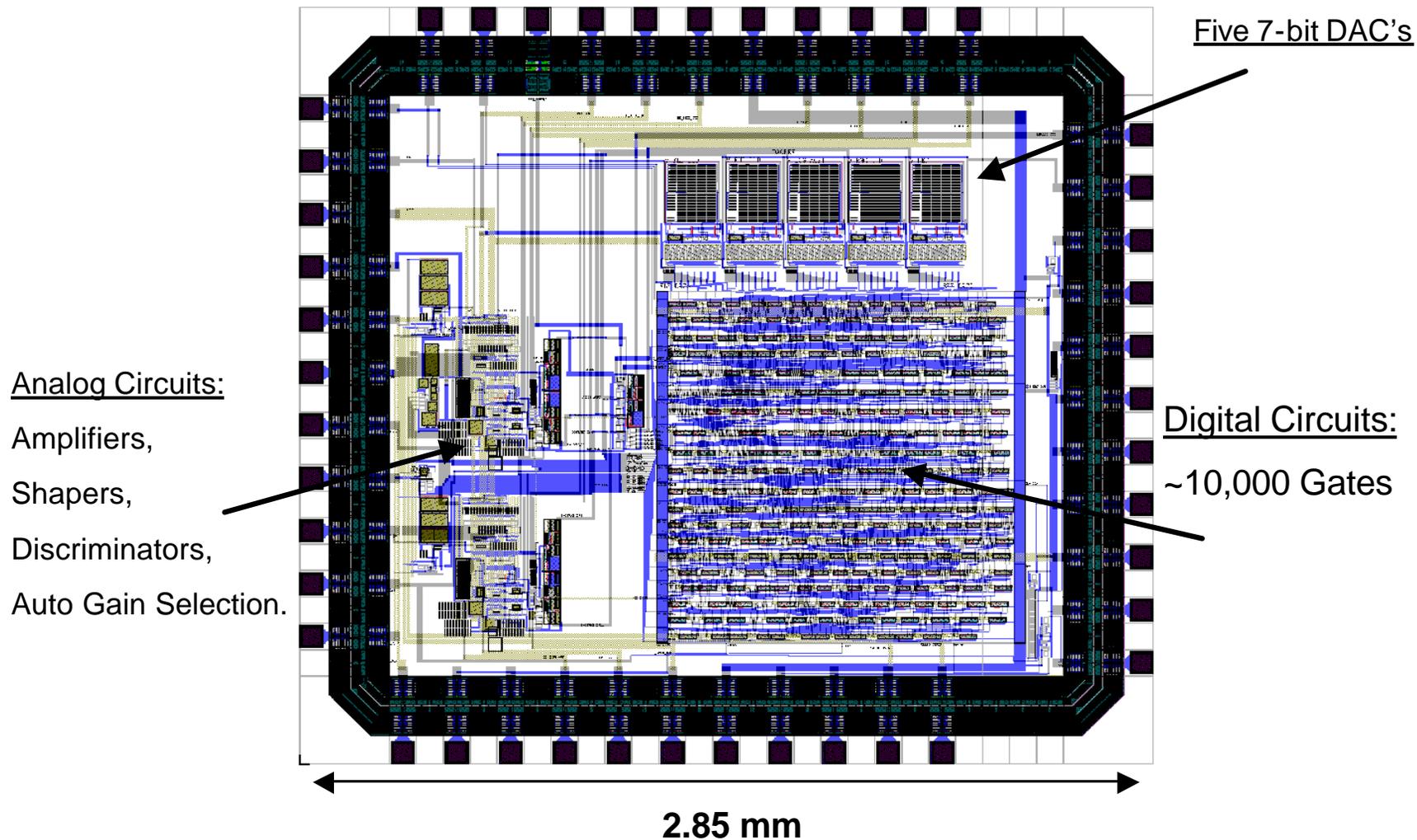
GCFE Simplified Block Diagram

- Analog signal path diagram shows four output ranges from two diode inputs





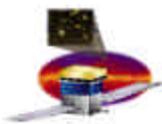
GCFE First Submission Layout





GCFE Status

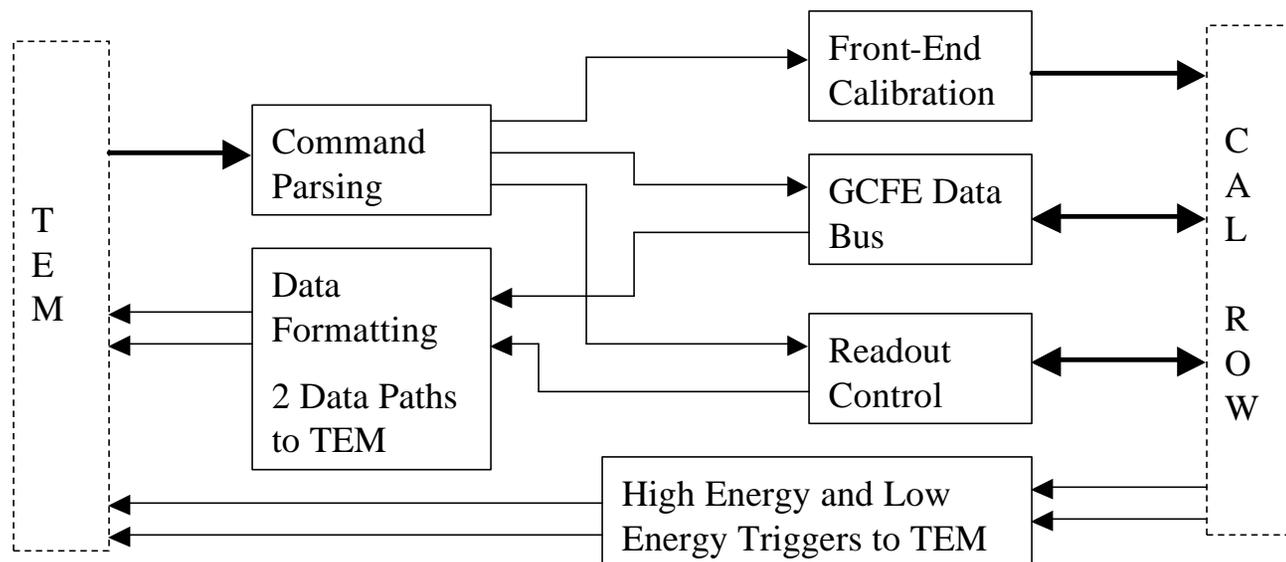
- ❑ First prototype GCFE1 received at SLAC in June 01
 - Contains all functionality
 - Analog: Multi-gain amplification, shaping, auto-range gain selection, trigger discriminators, five 7-bit DAC's
 - Digital: VHDL synthesized and auto place&routed digital circuits (~10,000 gates) for configuration/mode registers, write&read state-machine, data-acquisition state-machine & logic, etc.
 - Digital circuits fully functional, tested up to limit of test-box, 40 MHz, (f=20 MHz is nominal)
 - Capacitor-to-capacitor short of calibration-circuit to gain-selection circuit, found bug in linear capacitor extract software
 - Analog amplifier and shaper functional after cut of trace on chip
 - Single range calibration, charge-amplifier with external gain select, shaping, post-amplification, auto-ranging, acquisition sequence, rail-amplifiers, trigger discriminators are fully operational. Performance tests are in progress.
- ❑ 2nd Version GCFE2 received last week, has Single-Effect Upset hardened registers incorporated
- ❑ 3rd version GCFE3 with short fixed to be submitted July 28.



GCRC ASIC Block Diagram

□ GCRC Digital ASIC, main Features

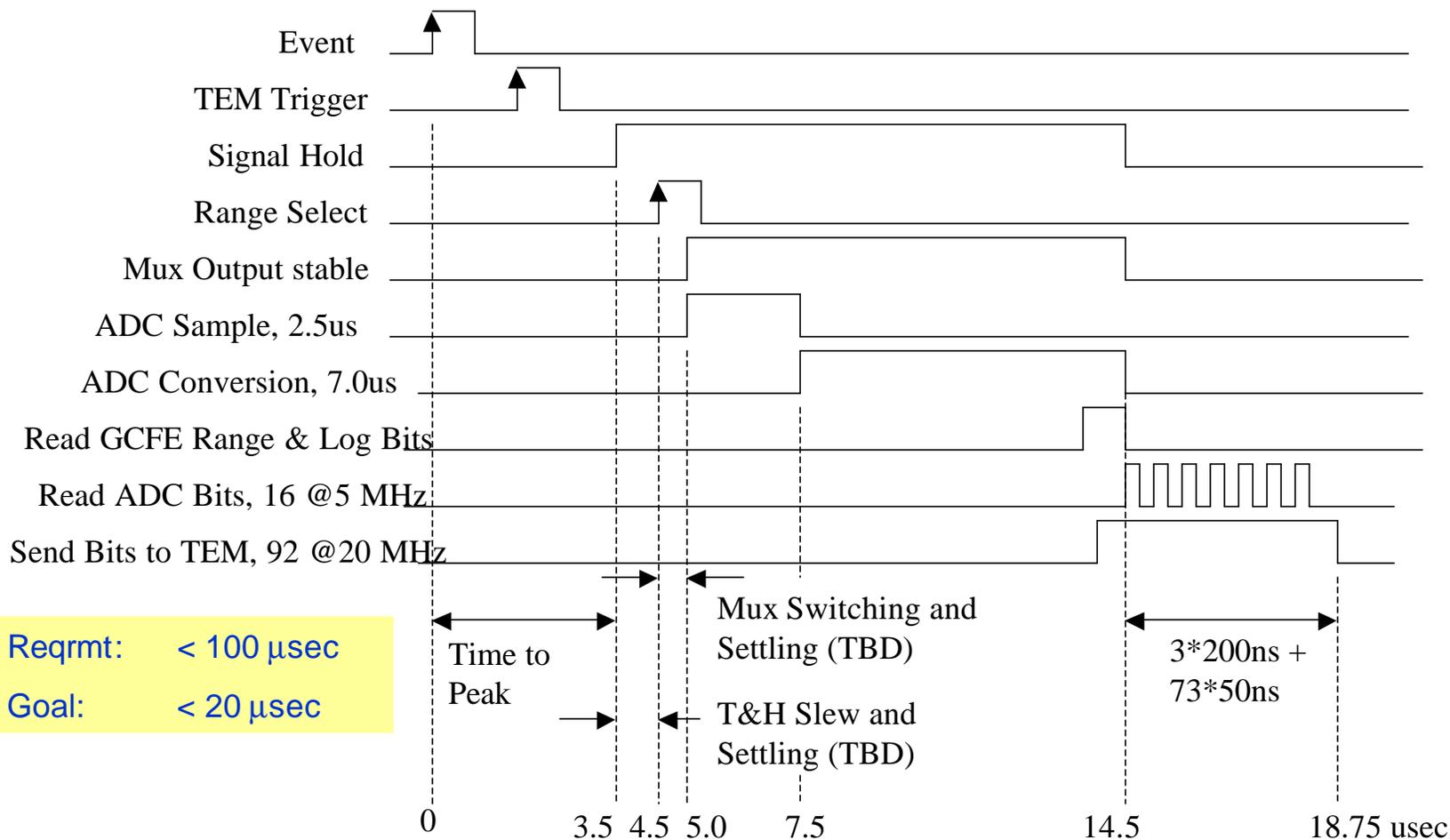
- 1 GCRC per Cal row interfaces 12 GCFE and 12 ADC chips to TEM
- LVDS communication used for all communication except ADC chips
- Each GCRC has a hard wired address to receive bussed commands from the TEM
- Targeted package 80 Pin Thin Quad Flat Pack 12mm square body



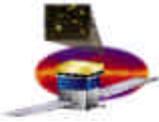


Readout Deadtime

- Shown below is a readout timing diagram, using Max145 ADC, internal conversion clock mode.

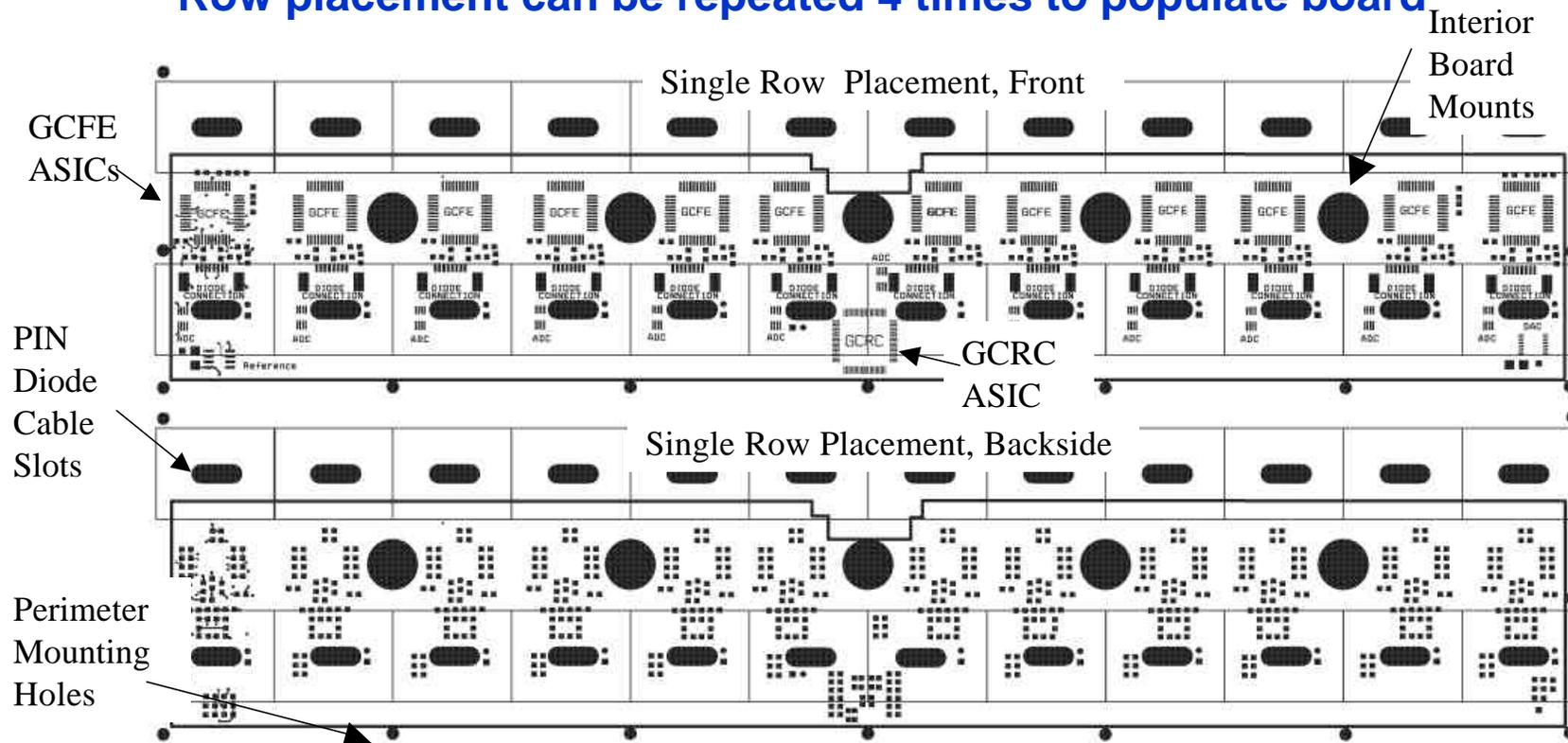


Reqmnt: < 100 μsec
Goal: < 20 μsec



Fitting of Design on PCB

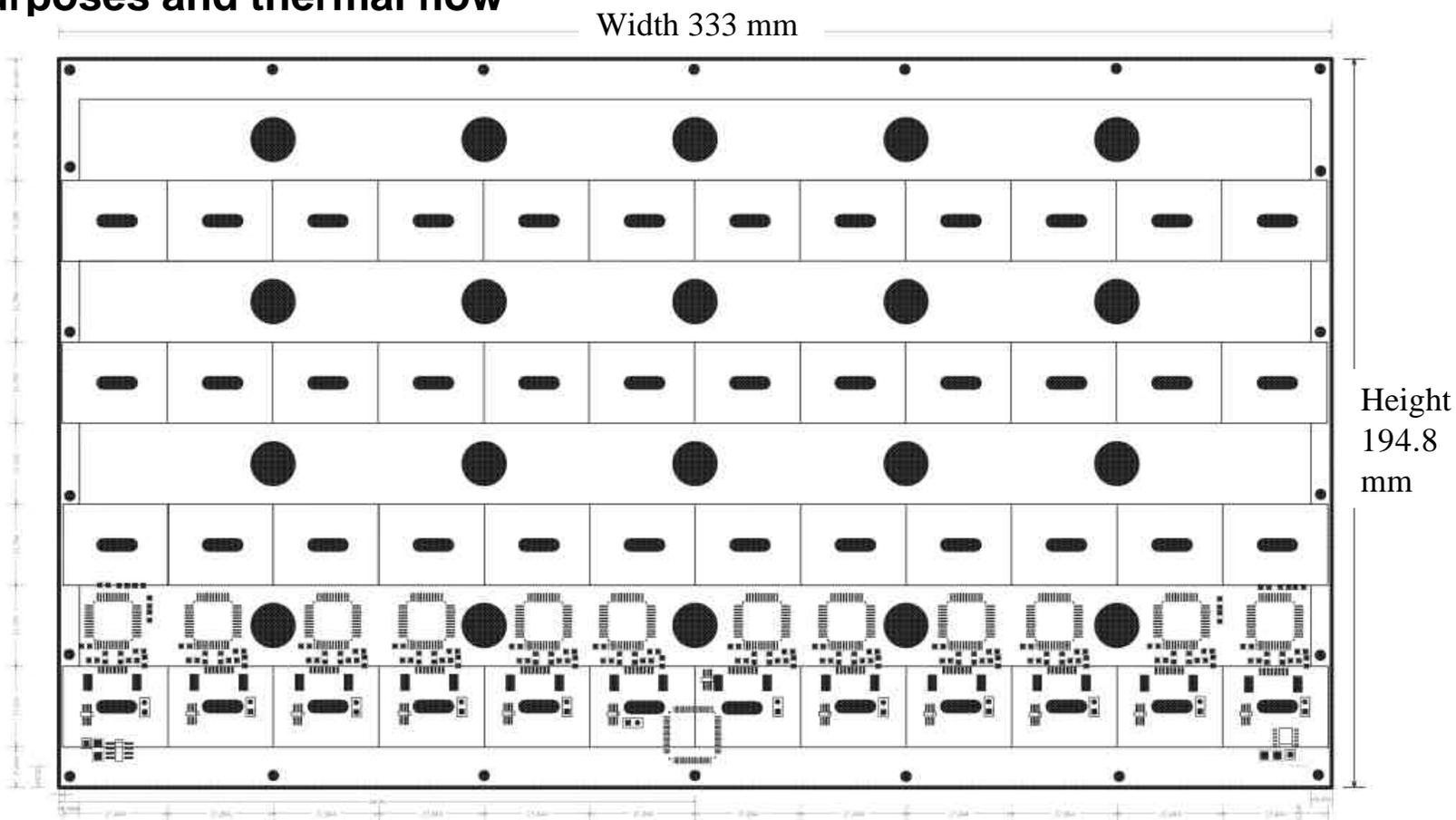
- ❑ Backside clearance reduced, more PIN diode clearance, thus only chip passive devices placed on bottom
- ❑ Single row placement shown below for bottom row
 - Row placement can be repeated 4 times to populate board





PCB, Full Side

- ❑ Full calorimeter circuit board showing bottom layer topside part placement
- ❑ All circuit board mounts connect to signal ground for grounding purposes and thermal flow

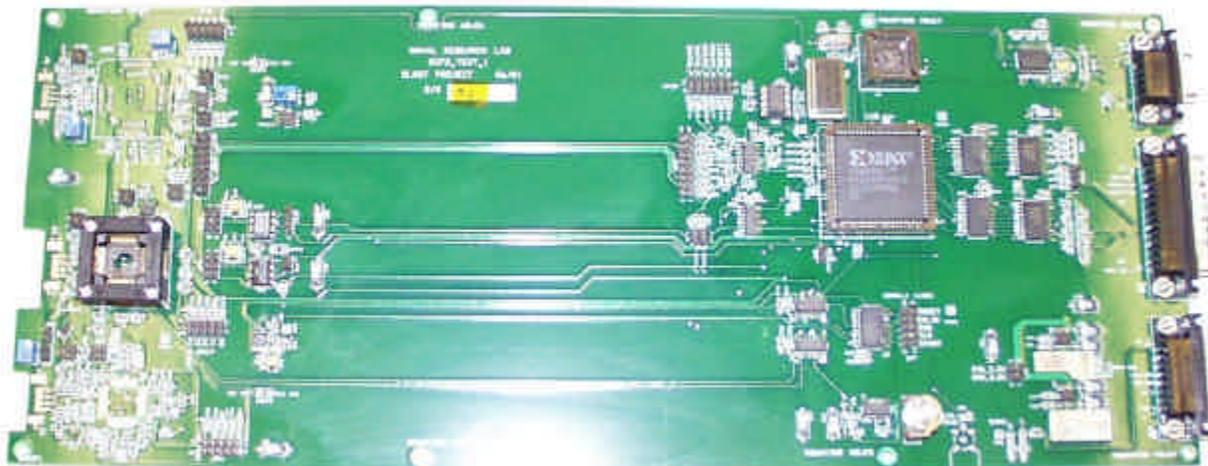




Analog ASIC Development

- ❑ Using HP 0.5um proven technology, second version ASIC received at SLAC 7/18/01
- ❑ NRL has built a GCFE Test Board to simulate use on flight board
 - Can be presently operated with digital pattern generator
 - FPGA coding and Labview software for test board control are being developed.
- ❑ NRL GCFE test system will also serve for radiation testing the chip
- ❑ Flight packaging will be plastic quad flat package
- ❑ Flight qualification and screening will be performed

NRL
GCFE
Test
Board





Digital ASIC Development

- ❑ Initial GCRC design will be tested in programmed FPGA device.
 - Presently designing GCRC Simulator board which will run GCRC design in Xilinx FPGA, and connect to GCRC ASIC footprint on Cal single row VM circuit board
- ❑ Upon GCRC design is thoroughly tested with the simulator on the Cal VM board, the design will be synthesized and fabricated in HP 0.5um silicon technology.
- ❑ Radiation testing will be performed on GCRC ASIC by NRL
- ❑ Flight qualification and screening will be performed



ADC Selection Matrix

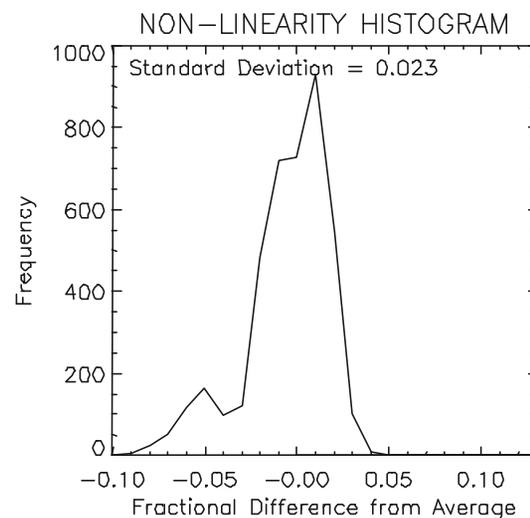
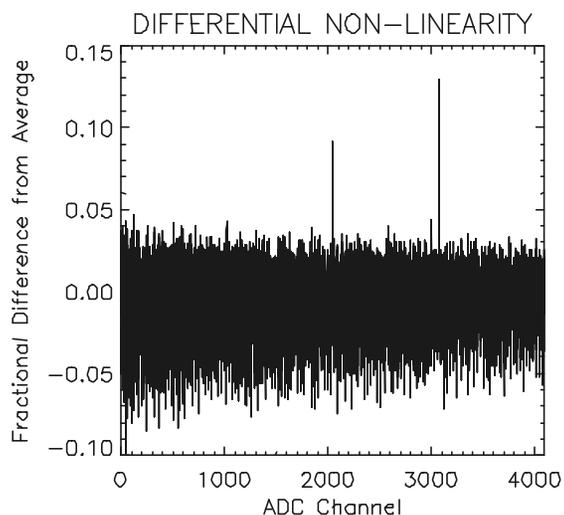
Devices of Most Interest

Parameter	Max189	AD7895	ADS7816	ADS8320	Max194	Max145	Max145	Max1241	AD7475
Smallest package	SO-16	SO-8	MSO-8	MSO-8	SO-16	MSO-8	MSO-8	SO-8	MSO-8
Number of bit resolution	12 bit	12 bit	12 bit	16 bit	14 bit	12 bit	12 bit	12 bit	12 bit
Operating voltage, Vdd, volts			4.5 – 5.5	2.7 – 5.2	+5 and -5	2.7 – 5.2	2.7 – 5.2	2.7 – 5.2	2.7 – 5.2
Wake-up time	2 us	5.7 us	0 us	0 us		2.5 us	2.5 us	4 us	0 us
Signal acquire time	1.5 us	0.3 us	1.0 us	1.8 us	2.6 us	2.5 us	2.5 us	1.5 us	0.135 us
Conversion Time	8.5 us max	3.8 us max	6.5 us	6.4 us (16 bits)	9.3 us (14 bits)	7 us	8us	7.5 us	0.625 us
Readout Time	3.5 us (4 MHz)	1.6 us (10 MHz)	0.5 us	0.4 us (2.5 MHz)	0 (1.5 MHz)	3.2 us (5 MHz)	0 (2 MHz)	6.25 us (2 MHz)	0 (20 MHz)
Total wake, convert & readout time	14.5 us	11.4 us	8.0 us	8.6 us	11.9 us	15.2 us	13.0 us	15.25 us	0.760 us
Power consumed in sleep (5V), max	15 uW	25 uW	15 uW	15 uW	100uW	25 uW	25 uW	75 uW	450 uW
Power consumed during conversion, (5V) typical	5 mW	16 mW	2 mW	3.25 mW	80mW	4.5 mW	4.5 mW	8 mW	9 mW
1KHz Rate power consumption, sleep mode between conversions	150 uW	300 uW	50 uW	500 uW		50 uW	50 uW	100 uW	500 uW
ADC clock	Internal	Internal	External	External	External	Internal	External	Internal	External
Input impedance	16 pF switched	0.5 uA max	25 pF switched	45 pF switched	250 pF switched	16 pF switched	16 pF switched	16 pF switched	20 pF switched
Input signal Range	0 to Vdd	0 to +3.5	0.1 to Vdd	0.5 to Vdd	0 to Vdd	0 to Vdd	0 to Vdd	1.0 to Vdd	0 to +2.5
Output data format	serial	serial	serial	serial	serial	serial	serial	serial	serial
12 bit Differential Non-Linearity, Standard Deviation	0.028		0.092	0.037	0.044	0.023	0.029	0.021	0.047 (10 MHz)
Laser Test Latchup Threshold, LET (MeV * cm ²)/mg	~ 70		15 - 20		~70			>150	30 - 40
Ion Beam Latchup Threshold, LET (MeV * cm ²)/mg	~60		<< 40		< 40	> 80	> 80	> 80	
SEU Upset Threshold, LET	~40		<< 40		<< 40	> 80	> 80	> 80	



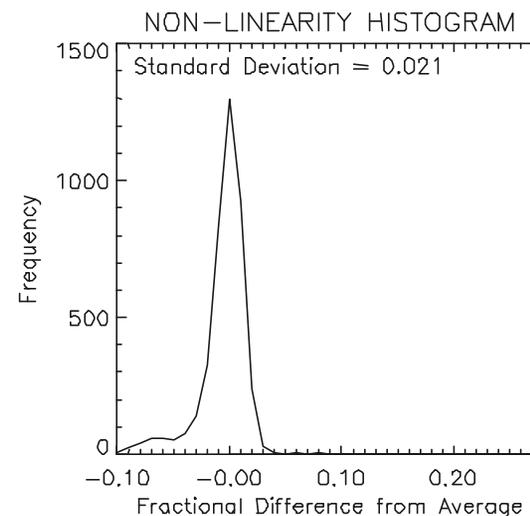
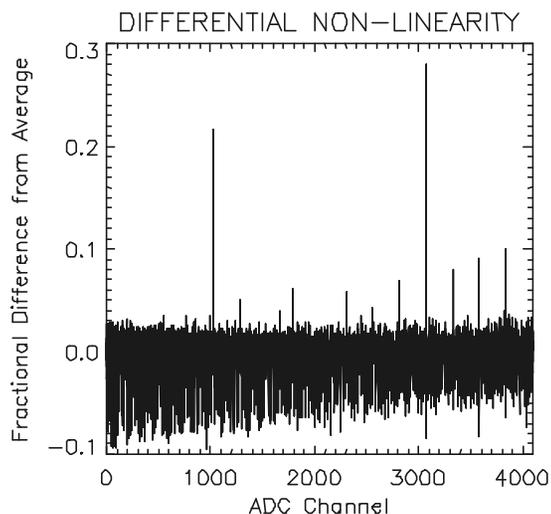
ADC Diff. Non-Linearity Testing

Maxim MAX145 12 bit ADC, Internal Conversion Clock, 12 bit DNL Plot.



Max145
Differential
Non-
Linearity
Plot

Maxim MAX1241 12 Bit ADC, 12 bit DNL Plot.



Max1241
Differential
Non-
Linearity
Plot



Challenges for EEE Parts Selection

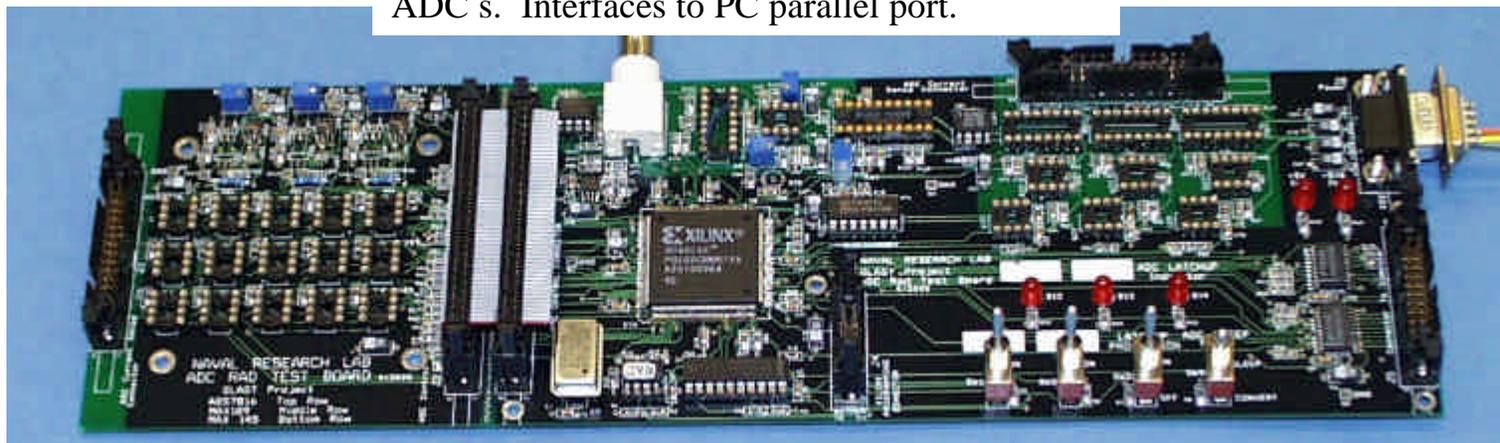
- ❑ No pre rad-hard 3.3V small outline package parts are available for design
 - 3.3V design requires newer generation of components which have generally not been test yet by others.
- ❑ ADC radiation testing resulted in two highly latchup immune devices
 - Maxim ADCs Max1241 and Max145 did not latchup at ion beam.
 - Tested up to gold beam at Brookhaven, 80 (MeV cm²)/mg
 - Very low upset rate at same energy levels.
 - Latchup sensitivity of 5 ADCs tested at Brookhaven corresponded well to laser latchup values measured at the NRL Radiation Test Facility.
 - Max1241 Laser latchup sensitivity measured > 150 (MeV cm²)/mg
- ❑ On track for radiation testing Digital to Analog Converters (DAC) and Op-Amps
 - Have 9 commercial 3.3V 12 bit DACs delidded for laser testing
 - Have 11 commercial 3.3V Op-Amps delidded for laser testing



Commercial Rad Hard, cont.

- Will perform total dose testing on selected parts
 - Do not expect total dose effects to be a problem on any devices
 - Expected total dose effects include:
 - ADC, worsening differential non-linearity
 - DAC, worsening integral non-linearity

ADC Radiation Test board. Tests 3 different ADC s. Interfaces to PC parallel port.





Commercial DACs, Op-Amps

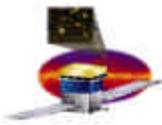
- Digital to Analog Converters (DACs) and Operational Amplifiers (Op-Amps) under consideration:

Manufacturer	DAC Part No.	Supply Volt	Bits Resolution	Data Format
Maxim	Max5121	3V	12	Serial
Maxim	Max5131	3V	13	Serial
Maxim	Max5133	3V	12	Serial
Texas Instruments	TLV5616	3V	12	Serial
Texas Instruments	TLV5636	3V	12	Serial
Texas Instruments	TLV5638	3V	12	Serial
Linear Technology	LT1453	3V	12	Serial
Linear Technology	LT1659	3V	12	Serial
Analog Devices	AD5320	3V	12	Serial

DAC
Table

Manufacturer	Op-Amp Part No.	Supply Volt	Input Range	Output Range
Maxim	Max4251	3 to 5V	Rail to Rail	Rail to Rail
Maxim	Max495	3 to 5V	Rail to Rail	Rail to Rail
Maxim	Max4123	3 to 5V	Rail to Rail	Rail to Rail
National Semi	LMC7101	3 to 15V	Rail to Rail	Rail to Rail
National Semi.	LM7301	3 to 30V	Rail to Rail	Rail to Rail
Texas Instruments	TLV2461	3 to 5V	Rail to Rail	Rail to Rail
Burr-Brown	OPA344	3 to 5V	Rail to Rail	Rail to Rail
Burr-Brown	OPA336	3 to 5V	Rail to Rail	Rail to Rail
Linear Technology	LT1218	3 to 15V	Rail to Rail	Rail to Rail
Linear Technology	LT1637	3 to 44V	Rail to Rail	Rail to Rail
Analog Devices	AD8541	3 to 5V	Rail to Rail	Rail to Rail

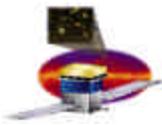
Op-Amp
Table



Diode Connect Requirements

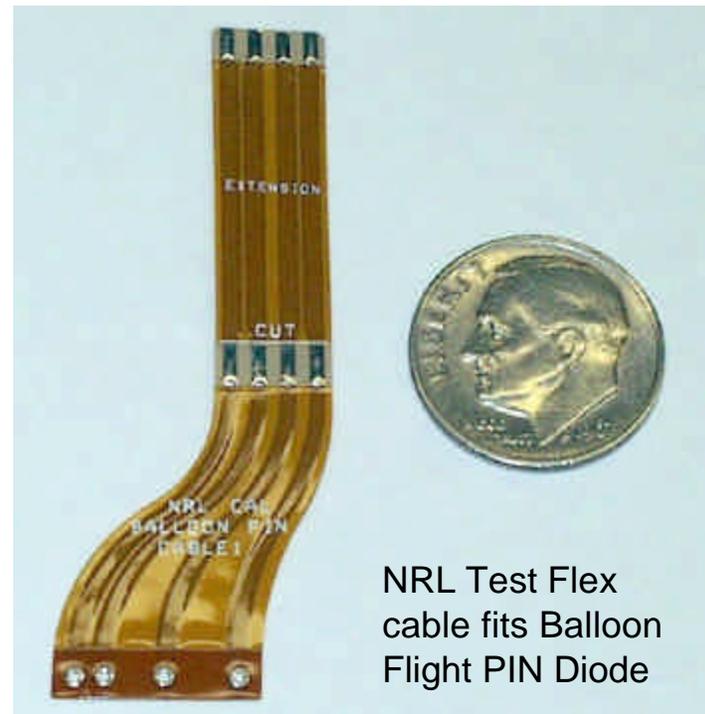
❑ PIN diode interconnect requirements

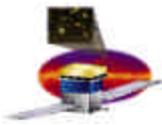
- 1) Connection not degrade the signal/noise ratio to the preamp
- 2) Maintain high impedance of diode signal connection
- 3) Low profile height off the diode ceramic carrier
- 4) Not be susceptible to picking up Electromagnetic Interference
- 5) Provide a means for testing the stacked crystals during flight assembly
- 6) Ability to adjust to alignment variations
- 7) Ability to adjust for crystal thermal expansion mismatch



PIN Diode Interconnect

- ❑ Flex circuit designed and tested as per IPC 6013 will be used for PIN Diode connection
- ❑ No shielding on cable will be used as per bread board testing at NRL
- ❑ Cable will have extra extension length for crystal stack testing
 - Extension will be sheared off for flight electronics connection





TEM Interconnect

- ❑ Flex cables used for Cal - TEM and Cal - Power connection.
- ❑ Connection of cable at TEM and Power made through qualified subminiature D connectors
 - Right angle through hole connectors will be mounted to flex cables
- ❑ Cable at Cal circuit board is built into board (qualified rigid-flex circuit board)
 - Benefits
 - Smoother PCB routing of signals off calorimeter board
 - More reliable connection than through pair of teeny Nanonics connectors
 - Rigid-flex design will be tested with Cal VM single row PCB fabrication.



Power

- ❑ Electronics designed for 3.3V power source
 - Analog circuits will have own supply for quieter operation
- ❑ Pin diode bias expect to operate around -70V, range -50 to -100V
 - Power draw is very low, rated load is for maximum estimated number of shorted flight diodes

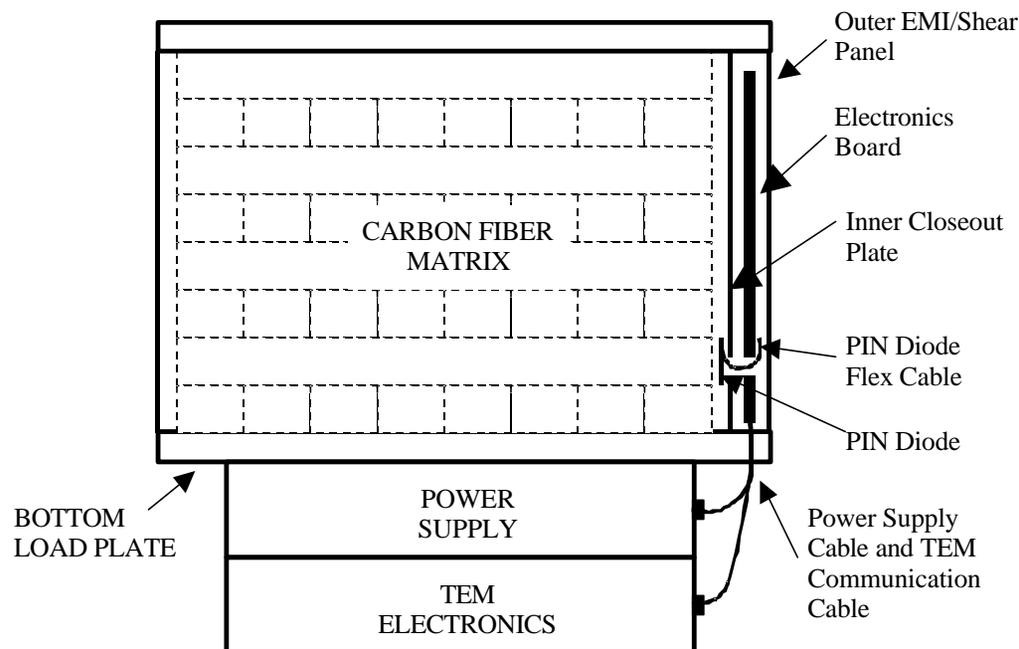
Conditioned Power Estimate

Item	Quantity	Power (mW)	
		Each	Total
GCFE	48	8	384
ADC Max145 (max)	48	4	192
Digital Controller ASIC	4	80	320
DAC	1	6	6
DAC Buffers	4	5	20
References	2	5	10
LV Biasing	48	1	24
PIN Bias	1	1	1
TOTAL Power per AFEE (mW)			957
TOTAL Power per Module (mW)			3,828
Allocated Power per Module (mW)			5,688



Grounding Plan

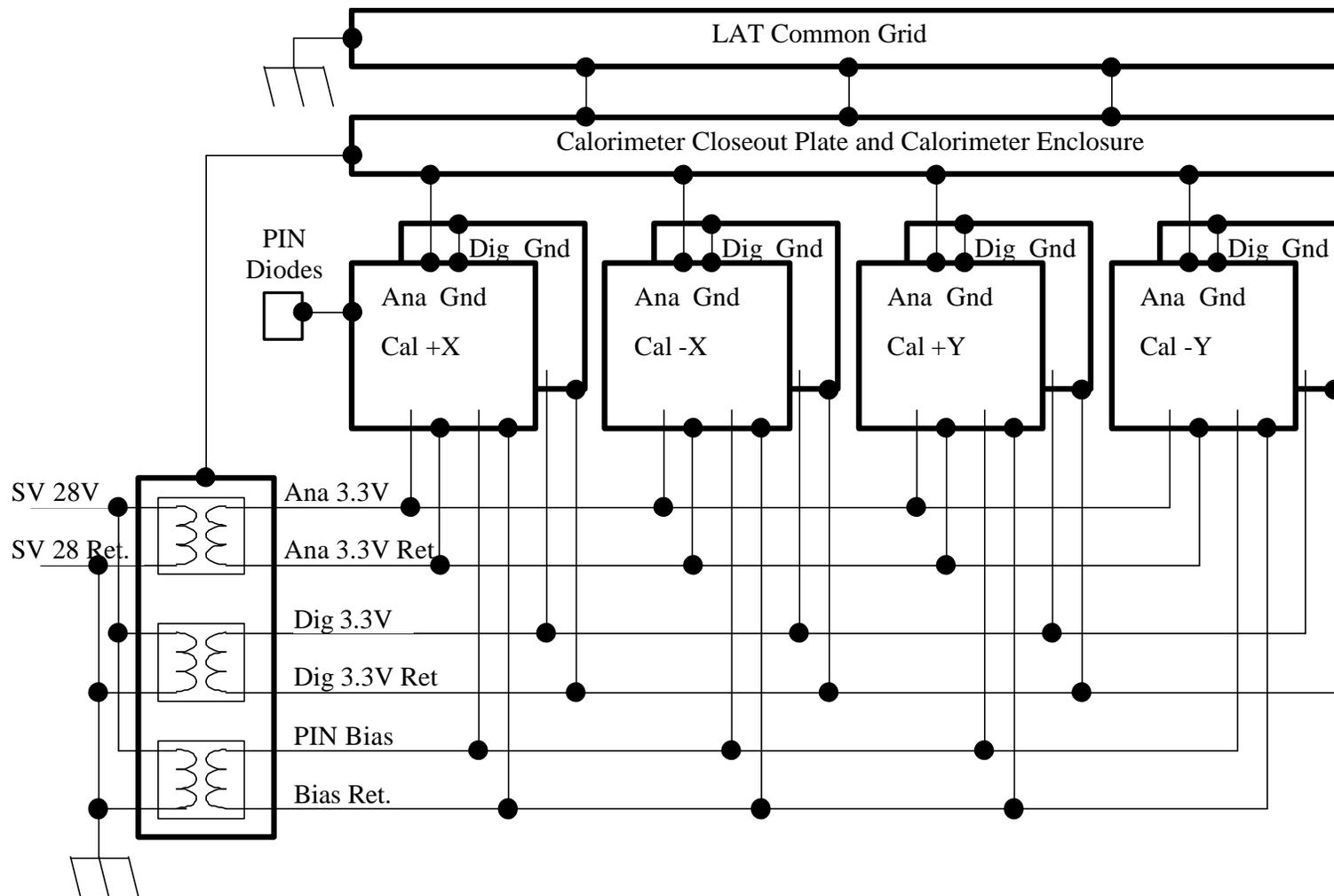
- ❑ For lowest noise operation, conductors near PIN diode must be referenced to same potential as the PIN diode.
- ❑ Therefore Calorimeter closeout plate is electrically connected to Cal circuit board signal ground and PIN diode is referenced to Cal circuit board signal ground.
- ❑ The Calorimeter structure/chassis is electrically connected to the closeout plate, thus the Cal structure is connected to signal ground

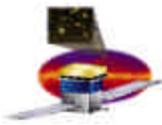




Grounding Diagram

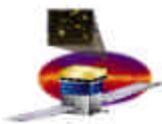
□ Calorimeter grounding block diagram is shown





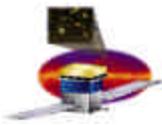
Cal Interfaces

- ❑ **Calorimeter Interface to TEM**
 - **Need to define TEM Cal Controller**
 - **Need to define signal connections and cable length to TEM**
- ❑ **Calorimeter Interface to Power Supplies**
 - **Need to define connections and cable length to Power Supplies**
- ❑ **Calorimeter electronics interface to calorimeter mechanical structure**
 - **Have tentative mechanical PCB interface, need to set circuit card mounting dimensions**
 - **Need to set closeout plate flex cable slots**



Parts List

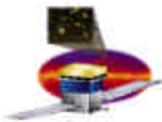
- ❑ Resistors from NPSL: Mil-R-55342, 1%, class S, RM1206, RM 0805 sizes
- ❑ Ceramic Capacitors from NPSL: Mil-C-55681, 5%, 50,100 volt, class S, CDR31, CDR32
- ❑ High Voltage Capacitors: 1000pF 200 volt, SMT packages, vendors under consideration
- ❑ Front End ASIC (GCFE) custom design, HP 0.5um process, 44 pin plastic quad flat pack package, possible packager ASAT, quantity 48 per board
- ❑ Readout Control ASIC (GCRC) custom design, HP 0.5um process, 80 pin plastic thin quad flat pack package, possible packager ASAT, quantity 4 per board
- ❑ ADC: Max145 or Max1241, manufacturer Maxim Integrated Products, 48 per board.
- ❑ DAC: TBR, 1 per board
- ❑ Op-Amp: TBR, 1 per board
- ❑ Reference: TBR, 1 per board
- ❑ Thermistor: 30K YSI (311P18-10S10R) or similar. Minimum 1 per board.
- ❑ PWB: polyimide rigid-flex printed circuit board per IPC-6012 and IPC-6013, Class 3, 100% netlist testing, coupon analysis.
- ❑ Connector MIL-PRF-83513 microminature connector, 2 per board
- ❑ Coating: Uralane 5750/5753



Issues

- ❑ **Issue of noise margin of custom LVDS signal communication**
 - **Need to test our custom LVDS circuitry for communication integrity.**
 - **Will use the GCFE Test Board and Cal VM Circuit board to verify the design**
 - **Expect same or similar LVDS driver/receiver designs to be used in both the GCFE and GCRC ASICs**

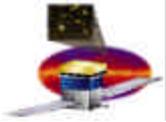
- ❑ **Issue of front-end noise performance in system**
 - **Need to determine and minimize front-end noise with calorimeter circuit board fully populated**
 - **Need to determine and minimize front-end noise with complete calorimeter assembled**



Issues (2)

- Issue of HP 0.5um process latchup susceptibility
 - ASIC designs are still to be tested for latchup
 - Expect similar latchup susceptibility of GCFE and GCRC
 - Literature [1] suggests normal cell designs in HP 0.5um process measured LET of approximately 63 (MeV cm²)/mg

 - Note: Total dose not expected to be a problem due to expected low lifetime accumulation of orbit and decreased total dose effects with lower voltage CMOS designs (thinner gate oxide). Literature [2] has reported HP 0.5um process measured N threshold shift of -40mV (10%) and P threshold shifts of 18mV (2%) at 100krad.
 - [1] Single Event Latchup Characteristics of Three Commercial CMOS Processes, J.V. Osborn et al., 7th NASA Symposium on VLSI Design, 1998
 - [2] Total Dose Hardness of Three Commercial CMOS Microelectronics Foundries, J.V. Osborn et al., IEEE Transactions on Nuclear Science, Vol. 45, No. 3, June 1998



CAL Module Assembly and Test

J. Eric Grove
Naval Research Lab



Assembly and Test Flow

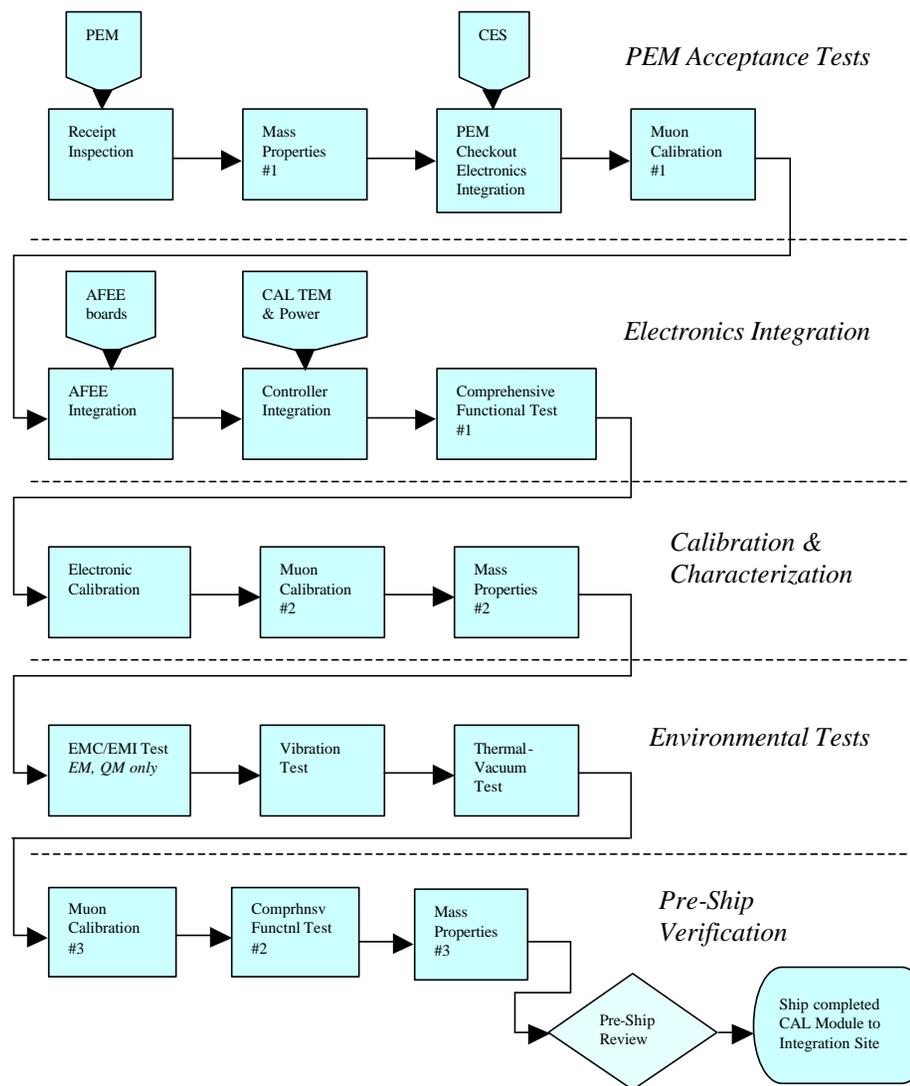
CAL Module Assembly and Test

Five stages of A&T sequence

- a) PEM acceptance tests
- b) Electronics integration
- c) Calibration, baseline
- d) Environmental tests
- e) Pre-ship verification

Sequence applies to all Modules, with some minor mods

Details in Module A&T Plan, LAT-SS-00262.





Assembly and Test Schedule

- Duration of assembly and test phases (working days for each Module)

Phase	Module			
	EM	QM, 1-2	3-6	7-16
PEM Acceptnce	14	9	8	5
Elect Integratn	25	14	10	9
Calibration	12	6	5	4
Environmental	28	17	11	11
Pre-ship Verifn	10	7	6	6
Margin	5	5	8	8
Total per Module	94	58	48	43

- Hardest challenges:
 - One PEM arrives at NRL every two weeks.
 - Five Modules in process at once.
 - One Module ships to LAT Integration Site (SLAC) every two weeks.
 - (but last Module arrives at SLAC five weeks before required date.)



Assembly and Test Schedule

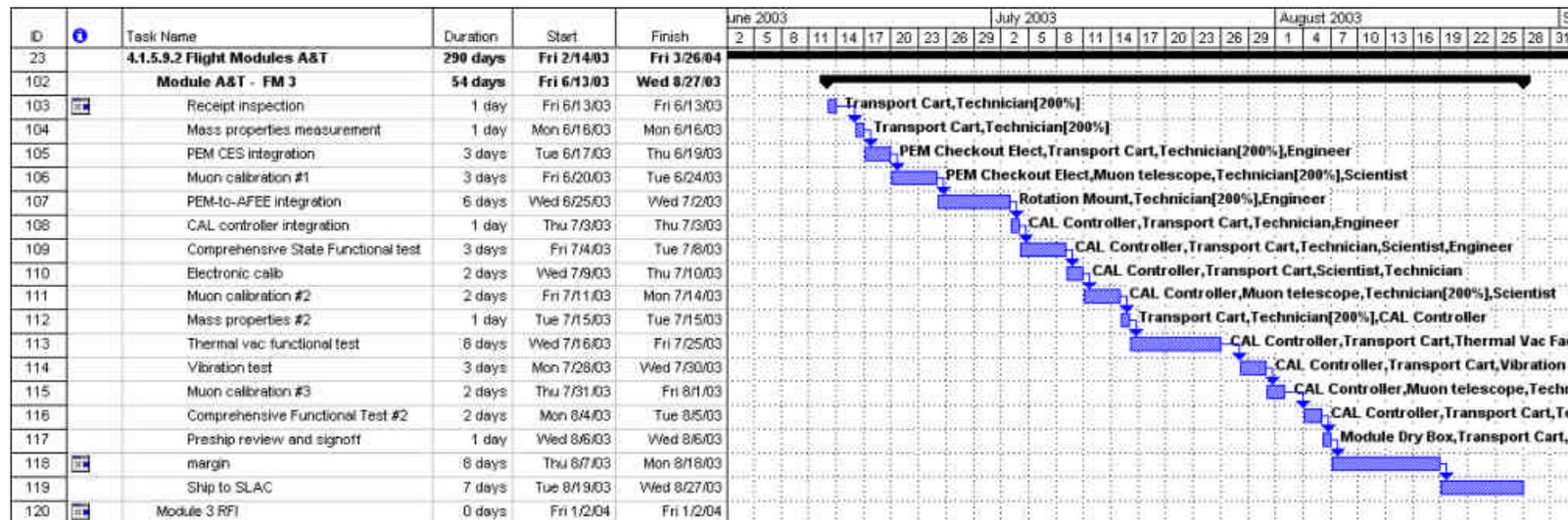
□ Delivery for integration into LAT

- Instrument integration schedule specifies required Ready For Integration (RFI) dates.
- RFI rate: Two Modules every two weeks.
 - Too much work in parallel, so we'll start earlier and stretch deliveries.
- Typical delivery rate: One Module every two weeks.
- Plan: FMs arrive at LAT Integration Site 5 to 18 weeks earlier than required.
 - Some margin for slippage.

Module	Planned Module Delivery Date	LAT Schedule Integration Date	Weeks delivery is early
Qual Model (FM A)	13 May 03	15 Aug 03	13
Flight Spare (FM B)	03 Jun 03	15 Aug 03	10
Flight Model 1	29 Jul 03	03 Nov 03	14
Flight Model 2	19 Aug 03	03 Nov 03	11
Flight Model 3	27 Aug 03	02 Jan 04	18
Flight Model 4	10 Sep 03	02 Jan 04	16
Flight Model 5	24 Sep 03	15 Jan 04	17
Flight Model 6	08 Oct 03	15 Jan 04	14
Flight Model 7	15 Oct 03	29 Jan 04	15
Flight Model 8	29 Oct 03	29 Jan 04	13
Flight Model 9	12 Nov 03	12 Feb 04	13
Flight Model 10	26 Nov 03	12 Feb 04	11
Flight Model 11	10 Dec 03	26 Feb 04	11
Flight Model 12	24 Dec 03	26 Feb 04	9
Flight Model 13	07 Jan 04	10 Mar 04	9
Flight Model 14	21 Jan 04	10 Mar 04	7
Flight Model 15	04 Feb 04	24 Mar 04	7
Flight Model 16	18 Feb 04	24 Mar 04	5



Assembly and Test Schedule

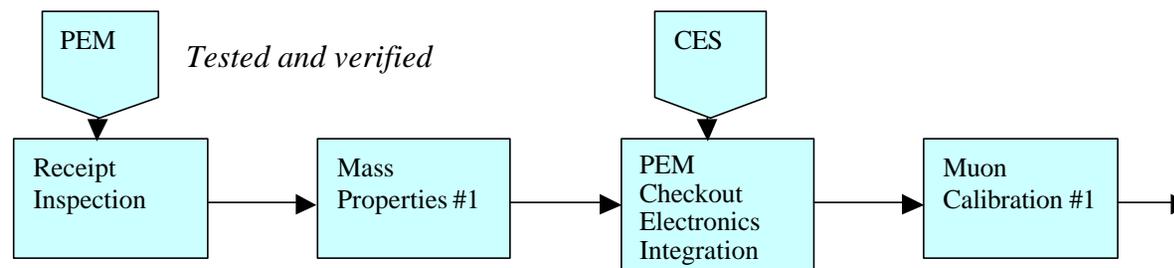


□ **Schedule for a single Module**

- **Average work crew per task per Module (full production, Modules 7-16)**
 - 1.7 technicians
 - 0.3 engineers
 - 0.5 scientists
 - Mission Assurance, admin support
- **Typical crew for a process**
 - Two technicians
 - One engineer or scientist
 - Mission Assurance, admin support



PEM Acceptance Tests



Receipt and Acceptance testing of PEMs

□ Goals

- Verify that PEM is undamaged, meets weight and dimensional specs, meets light yield and light attenuation specs

□ Inputs

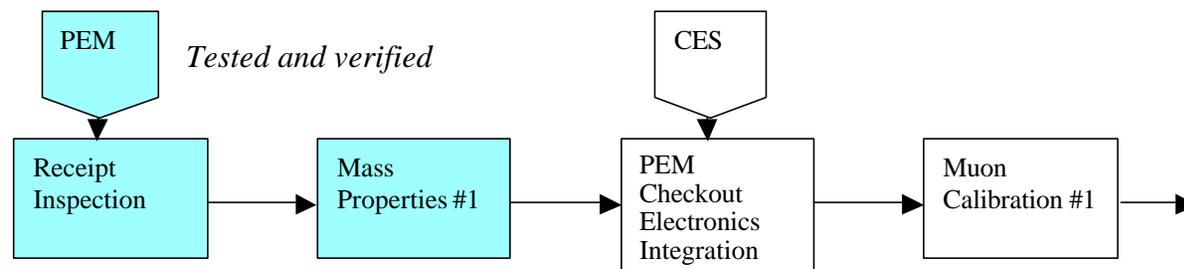
- PEM, fully tested and verified prior to shipment to NRL
- Data book for PEM
- Muon telescope
- Special EGSE: PEM Checkout Electronics System (lab electronics, DAQ)

□ Outputs

- Verified PEM
- Csl light yield and light attenuation maps



PEM Acceptance Tests



□ Receipt inspection

- Verify no visible damage in shipping, identity of PEM
- Data verification as per checklist
- Secure dry storage is available if the sequence queue is full

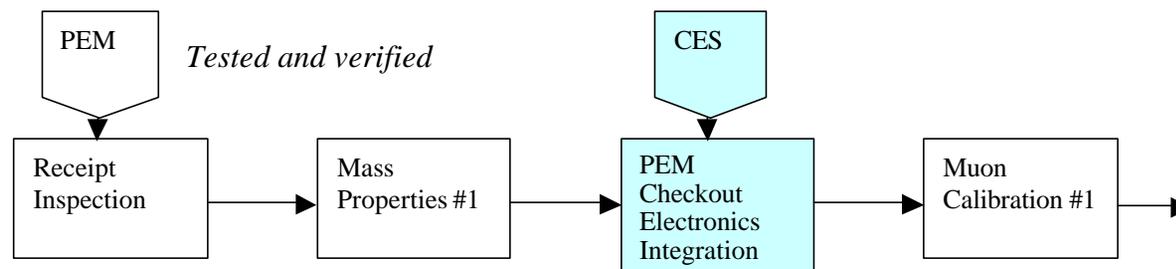
□ Mass properties measurement

- Measure weight and physical dimensions
- Verify compliance with requirements

- Throughout A&T sequence, all measurements, results, comments are entered in Module Properties Database, and Work Order is created or amended.

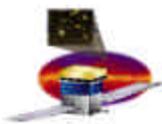


PEM Acceptance Tests

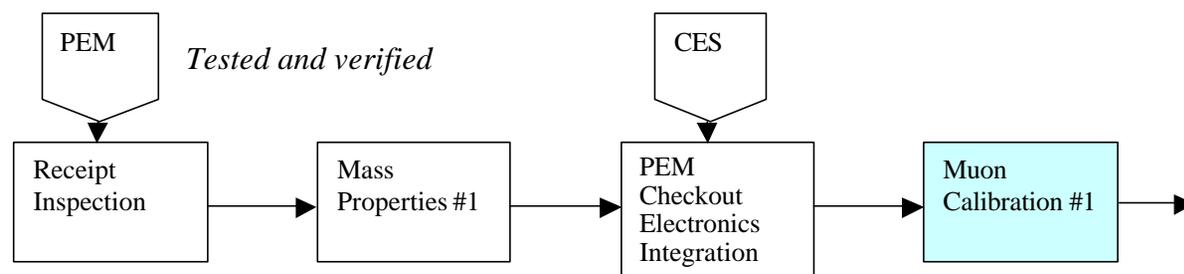


□ Checkout Electronics System integration

- Verifies optical performance of PEM before the flight electronics integration
- Lab analog and digital electronics and data acquisition for 192 channels
 - Hybrid preamps close to PINs. Very low noise.
 - Shaping amplifiers, discriminators (so self-triggering), ADCs.
 - Mechanical closeout provides EMI shielding.
- Prototype h/w and s/w developed for Beam Test Engineering Model (BTEM)



PEM Acceptance Tests



□ Muon calibration

- Requires muon telescope and PEM-CES
- Verifies quality of optical bonds and optical surfaces/crystal wraps
- Verifies scintillation light yield and light attenuation \Rightarrow science performance
- Calibration process:
 1. Collect ~1M muons.
 2. Image trajectories with telescope (i.e. dual wire chambers).
 3. Location and angle of incidence known for all xtals hit.
 4. Muons deposit known energy per unit pathlength (on average).
 5. Accumulate measured signal scaled for pathlength (S/sec θ) as a function of position along each xtal.
 6. Fit final muon peaks with Landau fcn (which describes fluctuation in energy loss for charged particles)
 7. Output is measured light yield and light attenuation.



Prototype of Checkout GSE

- ❑ Developed for assembly of BTEM
- ❑ **Prototype Muon Telescope**
 - Two 2D-position-sensitive multiwire proportional counters.
 - ~2 mm (rms) position resolution.
 - Mechanical support permitted crystal test box (shown) or complete BTEM calorimeter.
 - Preamps, shapers, trigger logic.
- ❑ **Prototype Checkout Electronics System**
 - 64 channels of preamps, shapers, discriminators, ADCs
 - PC-based data acquisition system. Software.

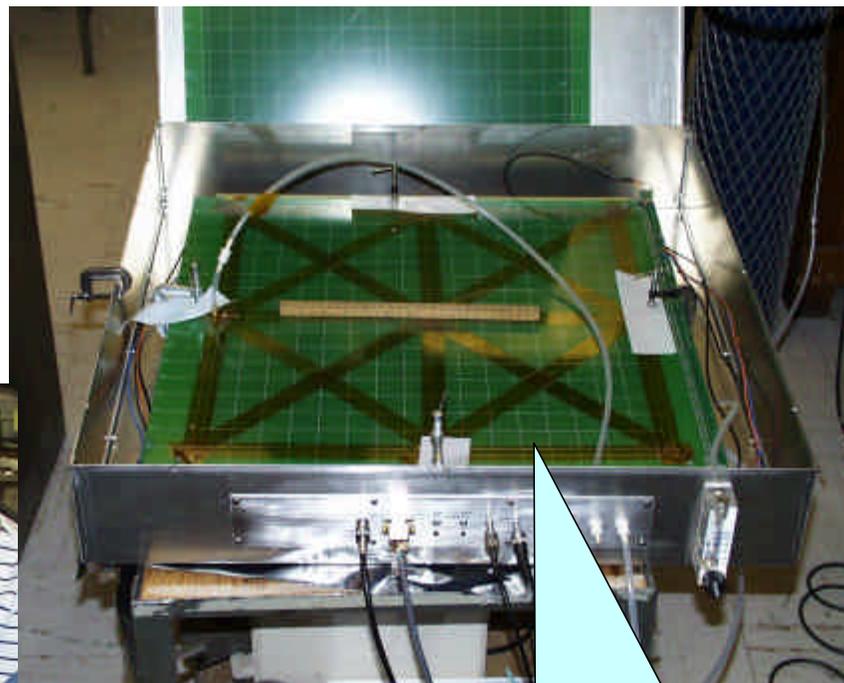


Muon telescope and
data acquisition system



PEM Checkout GSE

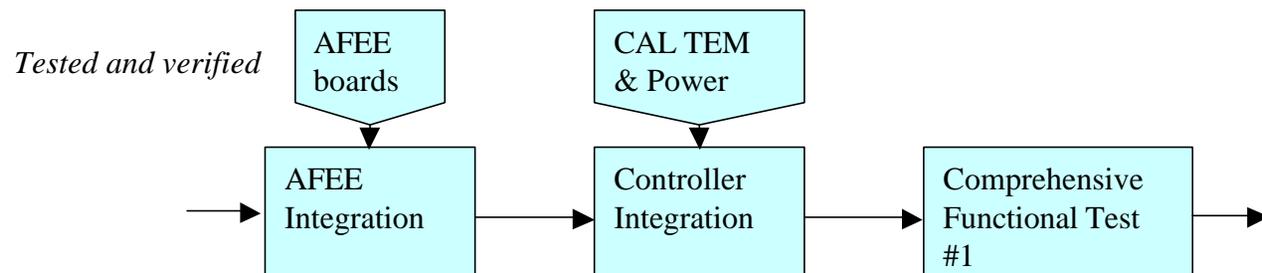
Prototype Checkout Electronics:
Front-end boards
(40-channel system)



Prototype Muon Telescope:
Wire chamber
(2-D position sensitive)



Electronics Integration



❑ Goals

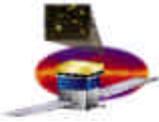
- Integrate flight front-end and controller electronics
- Establish baseline *system* performance

❑ Inputs

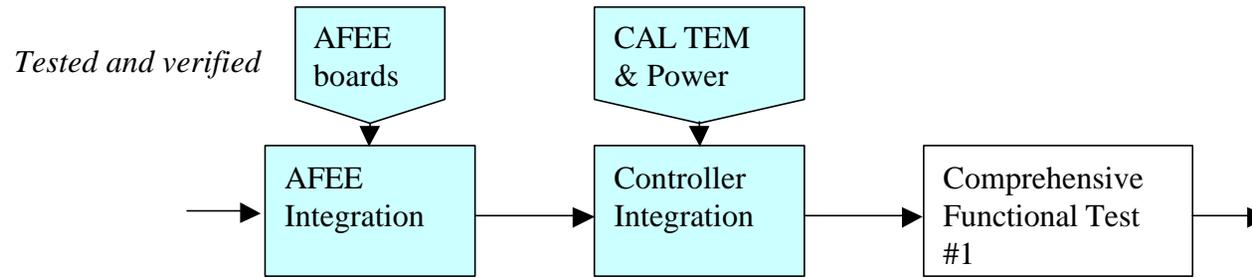
- Accepted PEM
- Flight AFEE boards, previously tested and verified
- Flight TEM, previously tested
- Flight (TBR) Power Supply, previously tested and verified
- Special GSE: Assembly/Rotation Stand, TEM Simulator, A&T Computer System

❑ Output

- Integrated, tested, fully functional CAL tower Module



Electronics Integration

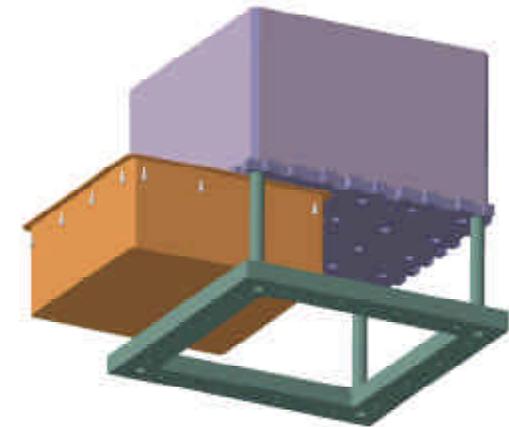


❑ Flight AFEE Integration

- Mechanical and electrical attachment
 - 48 flex circuits from PIN diodes to sockets per board
- Inspect by QA
- Test
 - Power-up aliveness, with lab PS
 - Limited functional, with TEM simulator (separately tested)

❑ Flight TEM and PS integration

- Mechanical and electrical attachment
- Test
 - Limited functional



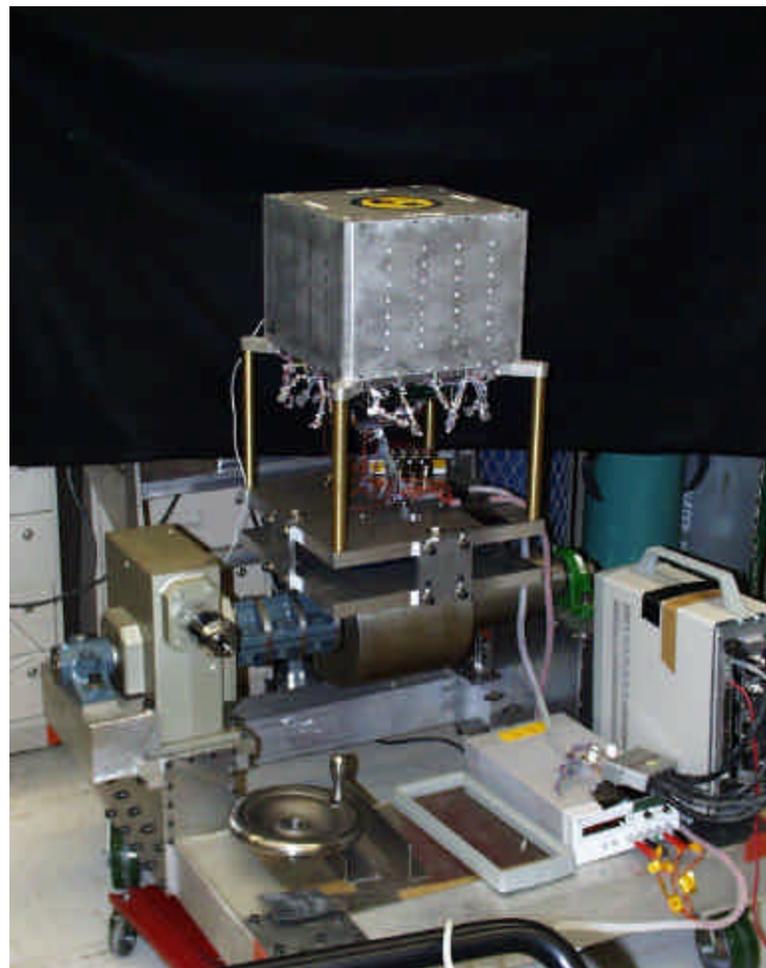


Electronics Integration

❑ Mechanical GSE

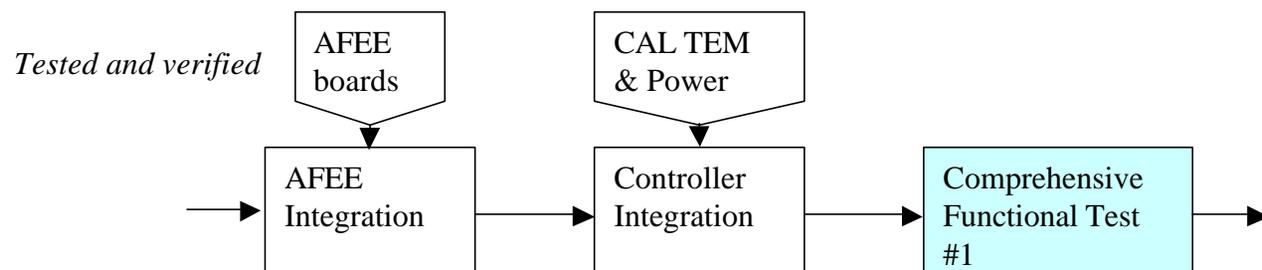
– Rotation / Assembly Stand

- Allows assembly tech and engineer easy access to each side of CAL in horizontal or vertical or any pitch.
- Prototype built for assembly of BTEM.





Electronics Integration

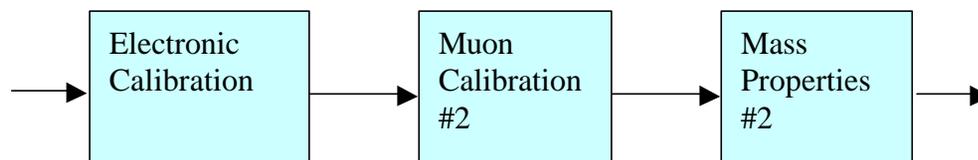


□ Comprehensive Performance Test #1

- Reference against which subsequent tests are compared
- Exercise and verify all
 - Commands
 - Data modes
 - Data channels, DACs, discriminators, ...
- Verify compliance with reqmts, acceptance standards
Calorimeter Performance Acceptance Standards and Tests (LAT-SS-00231)



Calibration & Characterization



❑ Goals

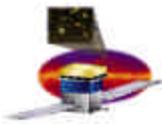
- Establish baseline gain and linearity of integrated Module.
- Establish weight, CM, and physical dimensions of integrated Module.

❑ Inputs

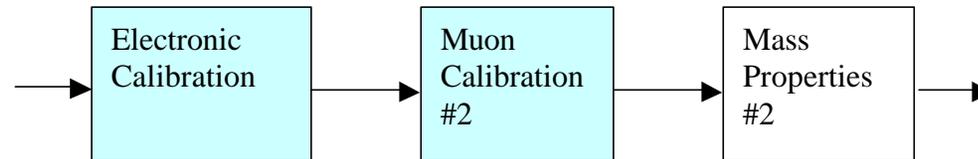
- Integrated and fully tested CAL Module with flight electronics.
- Special GSE: Muon telescope, A&T Computer System.

❑ Output

- 768 electronic gain and linearity curves per Module.
 - One for each energy range: 96 crystals \times 2 faces \times 4 ranges.
- 384 optical gains per Module.
 - One for each PIN: 96 crystals \times 2 faces \times 2 PINs.
 - Optical gain is electrons in FE per MeV deposited in xtal.
- Mass, CM, dimensions.
- Calibrated CAL Module.



Calibration & Characterization

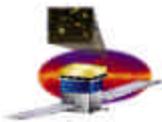


□ Electronic Calibration

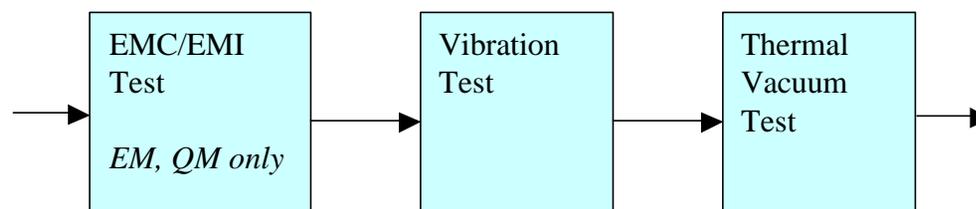
- Inject charge into each analog FE at 100 Hz rep rate, covering full dynamic range.
- Command sequence and analysis process extensively prototyped with BTEM.
- EGSE s/w creates calibration curves.

□ Muon calibration

- Repeat of previous test that used lab electronics.
- EGSE s/w creates light yields and light attenuation curves.
- Compare to PEM-CES response and known gain of AFEE.



Environmental Tests



□ Goals

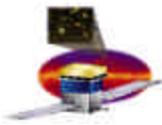
- Ensure Module safety and performance against thermal, pressure, vibration, shock, and electromagnetic excursions expected during flight.

□ Inputs

- Fully functional, calibrated CAL Module
- Thermal-vac, Vibration, EMC/EMI facilities
- Special GSE: A&T Computer System

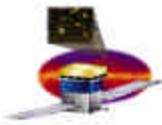
□ Outputs

- Qualified CAL Module



Environmental Tests

- ❑ **Electromagnetic Compatibility/Interference (EMC/EMI)**
 - **EM and QM**
 - **EMC/EMI testing of FM 1-16 and FS not required.**
 - **Verification by similarity**
- ❑ **Establishes neither source of EMI nor susceptible to EMI.**
 - **Tailored requirements from MIL-STD-461C/462C**
 - **Module powered, multiple configurations.**
 - **Measure EM signature in various modes.**
 - **LPT during external RF from facility emitters.**
 - **LPT after EMC/EMI tests completed.**
- ❑ **EMC/EMI facility at NRL will be used, along with experienced facility operators.**



Environmental Tests

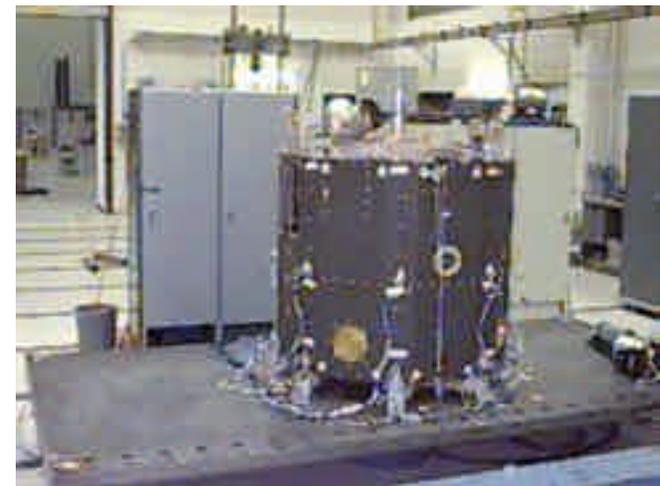
- ❑ **Vibration test**
 - EM, QM, FS: Qualification levels.
 - FM 1-16: Acceptance levels.

- ❑ **Modal survey**
 - 20 Hz – 2 kHz, 0.5 g
- ❑ **Sine-burst strength test**
 - Three-axis 15-g Qual, 12-g Accept
- ❑ **Random vibration test**
 - Comply with GEVS Table 2.4-4 and Appendix D, Table D-6 (Delta II)
- ❑ **LPT at conclusion of vibration test to confirm no degradation of performance.**
- ❑ **Visual verification of hardware.**

- ❑ **Vibration test facility at NRL will be used, along with experienced facility operators.**



Naval Center for Space Technology
Vibration Test Facility



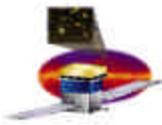


Environmental Tests

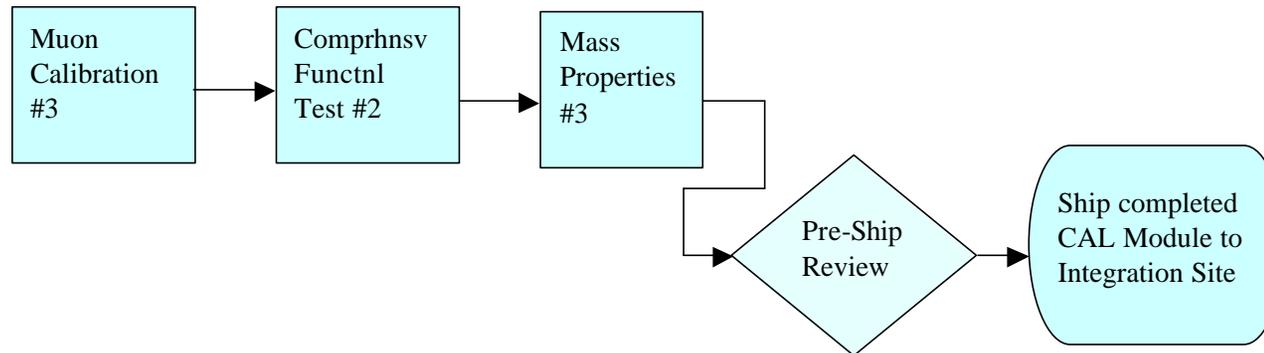
- ❑ Thermal-Vacuum tests
- ❑ Four thermal-vac cycles are required for each Module.
 - EM, QM (FM A), and FS (FM B) will cover Qualification range: -30C to +50C
 - FM 1-16 will cover Acceptance range: -20C to +40C
 - Gradient $dT/dt < 5C$ per hr (TBR), and soak time ≥ 2 hr.
 - Limited Performance Tests during one cycle, at plateaus and on slope.
 - LPT between and after cycling.
 - Must prevent condensation/hydration throughout setup and test. Procedural requirement.
 - Includes pressure profile test.
- ❑ Thermal-vac facility at NRL will be used, along with experienced facility operators.



Naval Center for Space Technology
Thermal Vacuum Facility



Pre-Ship Verification



□ Goals

- Final verification and qualification of Module for shipment
- Thorough pre-ship review

□ Inputs

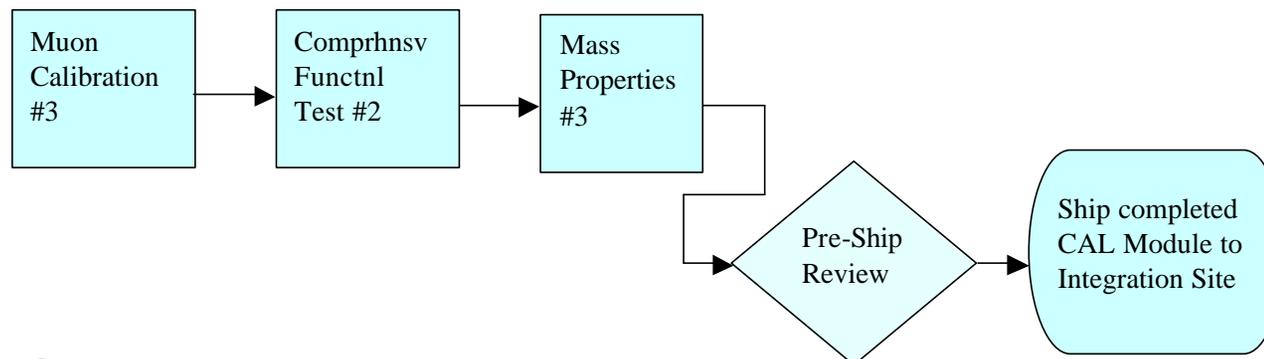
- Qualified CAL Module
- Special GSE: Muon telescope, A&T Computer System

□ Outputs

- Verified CAL Module ready for Integration
- Documentation!



Pre-Ship Verification



□ Final Testing

- Muon calibration establishes final optical gain and light attenuation.
- CPT establishes full functionality.
- Mass properties measurement establishes final compliance with weight and dimensions.

□ Pre-Ship Review (Integration Readiness Review)

- Review Board consists of Subsystem Manager, A&T Manager, Systems Engineer, QA Engineer, Lead Engineers, others as deemed necessary.
- Walk-through A&T flow, review Test Reports, Resolution Reports, status of all anomalies, etc.

□ The Module and TEM must satisfy CAL Performance Acceptance Standards and Tests (LAT-SS-00231).



Verification Matrix

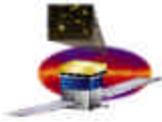
LEVEL	COMPONENT (ITEM)	HARDWARE			MECHANICAL							ELECTRICAL					THERMAL				OTHER					COMMENTS
		QUANTITY	TYPE	SUPPLIER	STATIC LOAD	SINE BURST	SINE SWEEP	RANDOM VIB	ACOUSTIC	PRESSURE PROFILE	MASS PROPERTIES	INTERFACE VERIF	EMC/EMI	ESD COMPATABILITY (GNDING)	MAGNETICS	FUNCTIONAL	THERMAL VACUUM	THERMAL BALANCE	THERMAL CYCLE	HUMIDITY	RADIATION	BAKEOUT	BEAM TEST - EM SHOWERS	BEAM TEST - HADRONS	BEAM TEST - HEAVY IONS	
C	VM2 Csl Det Elements (CDE)	12	Q	F	A			A			M	T	A	A	A	T	TQ		TQ		T					
C	VM2 PreElect Modules (PEM)	1	Q	F	T	TQ	TQ	TQ		TQ	M	T				T	TQ		TQ		T					
C	VM Electronics Prototype	1	Q	N												T										
	EM Csl Det Elements (CDE)		Q	F	T	TQ	TQ	TQ			M	T				T	TQ		TQ		M	TQ				TQ applies to sample batches
C	EM PreElect Modules (PEM)	1	Q	F	M	TQ	TQ	TQ		TQ	M	T				T	TQ		TQ		M		A			
C	EM Front End Elect (AFEE)	4	Q	N	A	A	A	A			M	T	A	A	A	T	TQ		TQ		M	A	A			
S	EM CAL Module	1	Q	N		TQ	TQ	TQ			M	T	T	T	T	T	TQ		TQ		M	A	A	T	T	T
	QM Csl Det Elements (CDE)		Q	F	T	TQ	TQ	TQ			M	T				T	TQ		TQ		M	TQ				TQ applies to sample batches
C	QM PreElect Modules (PEM)	1	Q	F	M	TQ	TQ	TQ		TQ	M	T				T	TQ		TQ		M		A			
C	QM Front End Elect (AFEE)	4	Q	N	A	A	A	A			M	T	A	A	A	T	TQ		TQ		M	A				
S	QM CAL Module	1	Q	N		TQ	TQ	TQ			M	T	T	T	T	T	TQ		TQ		M	A	A			
	FM Csl Det Elements (CDE)		F	F		TQ	TQ	TQ			M	T				T	TQ		TQ		M	TQ				TQ applies to non-flight samples
C	FM PreElect Modules (PEM)		F	F	M	TA	TA	TA		TA	M	T				T	TA		TQ		M		A			
C	FM Front End Elect (AFEE)		F	N	QS	QS	QS	QS			M	T	QS	QS	QS	T	QS		TQ		M	A				
S	FM CAL Module	17	F	N		QS	QS	TA			M	T	QS	QS	QS	T	TA		TQ		M	A	QS			

Calorimeter Verification plan & Environmental Specification, TBD
System Level Electrical Requirements, TBD
Contamination Control Plan, TBD
Grounding checked for each component prior to S/C integration

LEVEL OF ASSEMBLY:
S = Subsystem
C = Component
SUPPLIER:
F = France
N = NRL

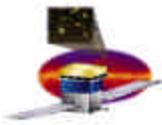
UNIT TYPE:
PF = ProtoFlight
F = Flight
S = Spare
Q = Qual. unit

VERIFICATION METHOD:
T = Test
A = Analysis
M = Measurement
I = Inspection
QS = Qual by Similarity
TQ = Test, Qual level
TA = Test, Acceptance level



LAT Calorimeter Safety & Mission Assurance

Nick Virmani
NRL / Swales



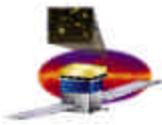
Safety & Mission Assurance

General

- ❑ The Calorimeter S&MA Program will be conducted in accordance with LAT PAIP, SLAC LAT-MD-00039-1.
- ❑ Lessons learned from other programs will be utilized.
- ❑ Calorimeter ground data systems program will be developed in accordance with the LAT PAIP.
- ❑ The implementation relies upon the controlled application of procedures, instructions and integrated product teams.

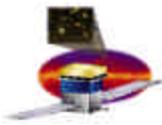
Objectives

- ❑ Design it to specifications the first time.
- ❑ Build it correctly the first time.
- ❑ Procure quality compliant parts.
- ❑ Test it completely the first time.



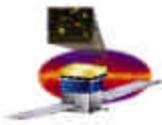
System Safety Program

- ❑ **The Calorimeter safety program will be in accordance with the LAT System Safety Program Plan, SLAC LAT-MD-00078-01.**
- ❑ **Will support GSFC and LAT for assessment of orbital debris and acceptable level of risk.**
- ❑ **Will perform hazard analysis and risk mitigation.**
- ❑ **Will identify and control hazards to personnel, facilities, support equipment, and flight hardware during all stages.**



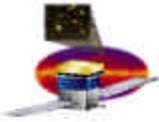
EEE Parts Program

- ❑ **EEE Part Program Control Plan LAT-MD-00099-02 implemented.**
- ❑ **CAL design engineers will use Quality Level 2 parts per GSFC-311-INST-001 which governs the selection, screening, and qualification processes.**
- ❑ **Parts selection process will utilize the NASA Parts Selection List (NPSL), MIL-STD-975, GSFC PPL-21, and DESC QML P/N.**
- ❑ **All EEE parts will be derated in accordance with PPL-21 and stress analysis performed to compare against the nominal stress derating criteria.**
- ❑ **Parts Control Board (PCB) manages parts activities.**
- ❑ **PCB will verify that all parts meet requirements of radiation, parts heritage, quality level, specifications, upscreens, DPA, other tests, and source inspections.**
- ❑ **Component / Subsystem / System Engineers will generate parts list and submit to PCB for approval. Separate list for parts, materials and processes will be prepared.**

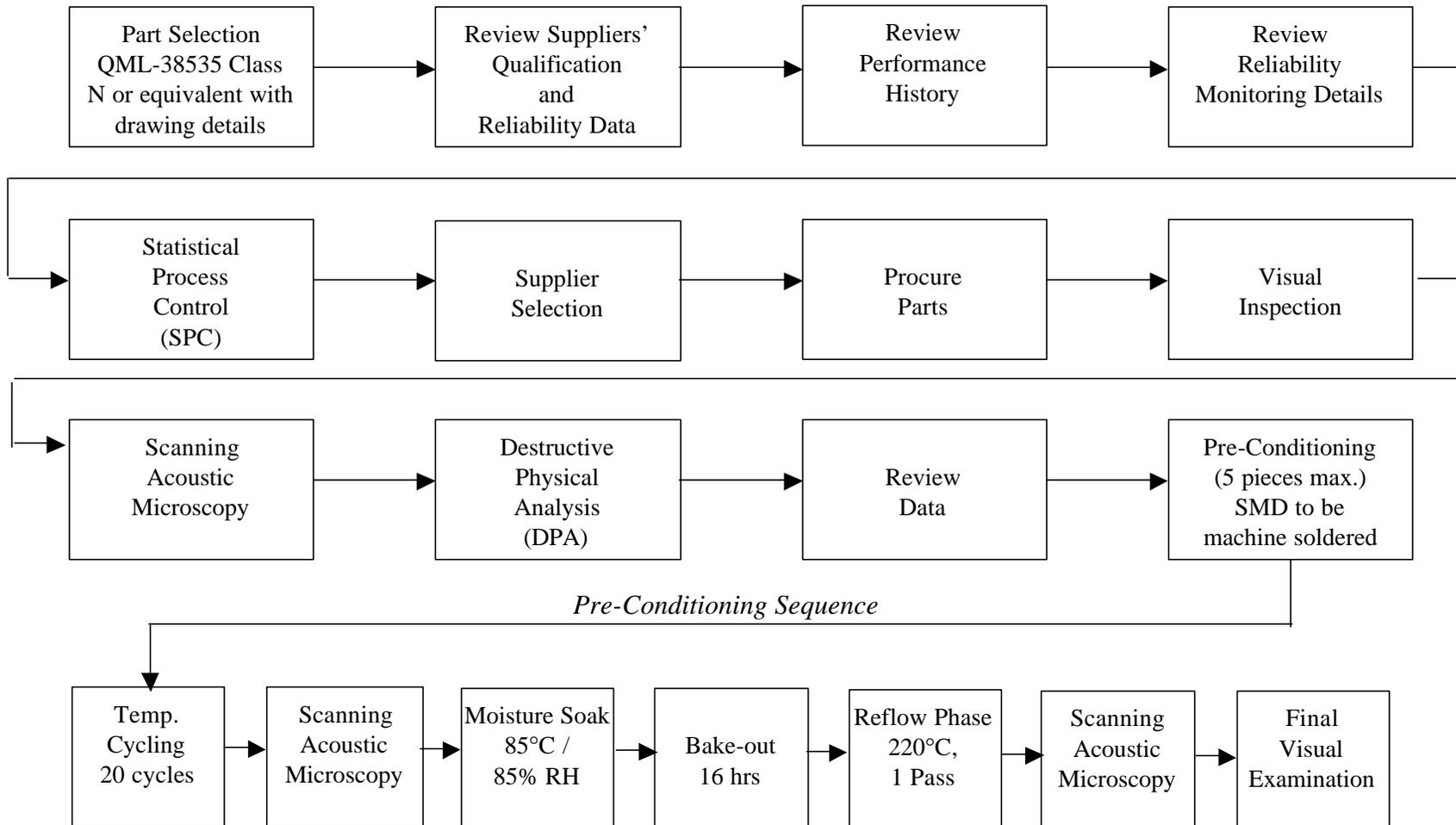


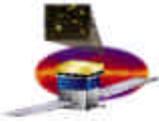
EEE Parts Program (cont)

- ❑ PCB determines the acceptability of heritage parts and the need for preparation of SCD's, specifications or waivers for non-MIL, non-NPSL qualified parts on an as-needed basis
- ❑ Non-QML, non-NPSL will be supported by up-screening and/or qualification procedure detailed in the parts program plan.
- ❑ At present, focusing on long lead active parts including ASIC, DAC, PIN Photodiodes, etc.
- ❑ Specific EEE parts requirements will be addressed by subsystem leads.
- ❑ Procurement strategy being identified and orders will be placed.
- ❑ Plastic Encapsulated Microcircuits (PEMs) will be used where equivalent hermetic sealed and qualified parts are not available.
- ❑ PEMs will be qualified and screened as per flow diagram and SCD.

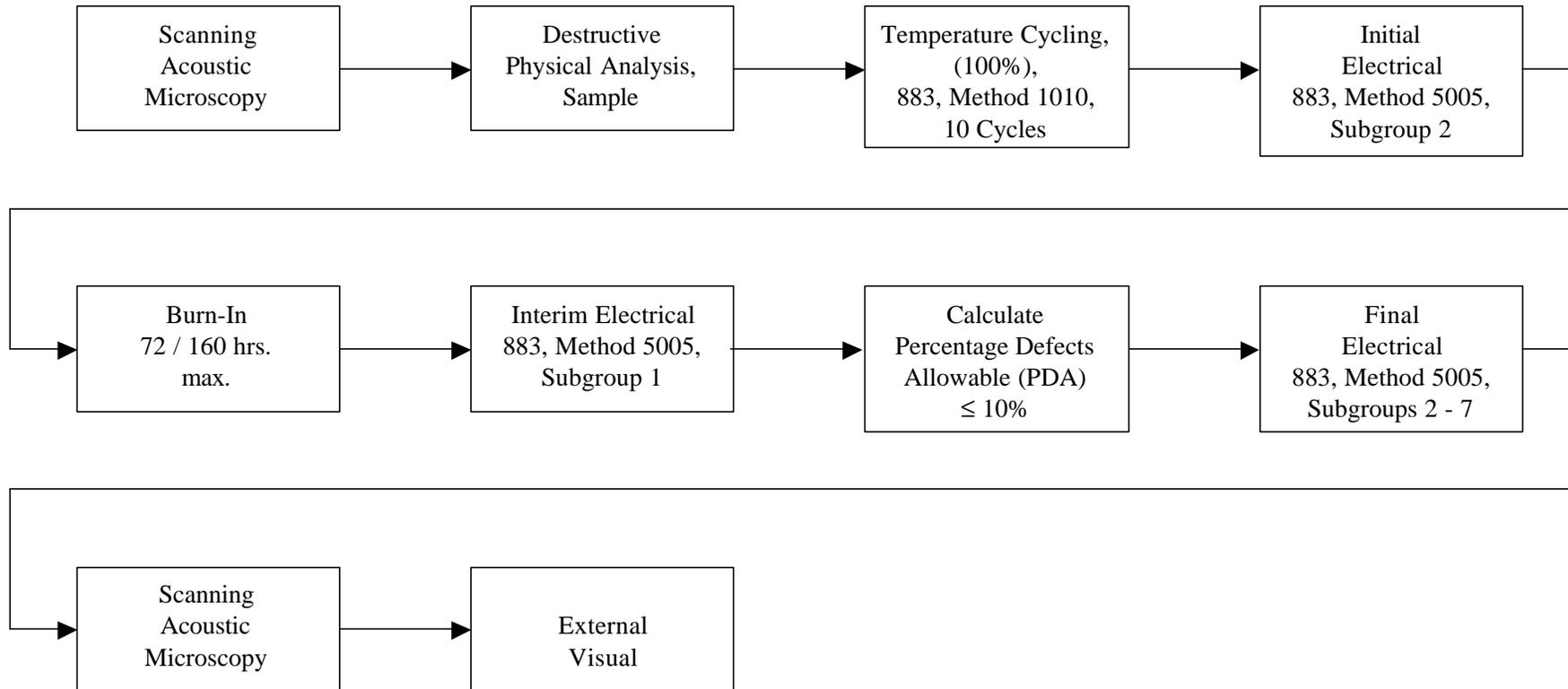


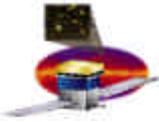
Qualification and Validation of Plastic Encapsulated Microcircuits (PEMs)





Plastic Encapsulated Microcircuits (PEMS) Screening (100%)

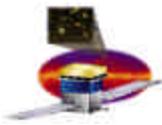




Packaging, Manufacturing, Test and Process Control

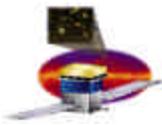
Manufacturing, Assembly, and Quality Control of Electronic System will be in compliance to the following NASA technical standards:

- [NASA-STD-8739.1](#) **Workmanship Standards for Staking and Conformal Coating of Printed Wiring Boards and Electronic Assemblies**
- [NASA-STD-8739.2](#) **Workmanship Standard for Surface Mount Technology**
- [NASA-STD-8739.3](#) **Soldered Electrical Connections**
- [NASA-STD-8739.4](#) **Crimping, Interconnecting Cables, Harness, and Wiring**
- [NASA-STD-8739.7](#) **Electrostatic Discharge Control**
- [IPC-6012 & IPC-6013](#) **Rigid and Flexible PWBs**



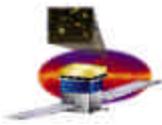
Packaging, Manufacturing, Test and Process Control (cont)

- ❑ **PWB Coupon will be analyzed prior to flight assembly.**
- ❑ **Particular attention will be paid to the quality of workmanship, soldering, welding, wiring, marking of parts and assemblies, plating and painting.**
- ❑ **Verification of flight hardware will be performed by NASA certified and qualified personnel other than the original operator.**
- ❑ **An item inspection will be performed on each component to verify:**
 - **Configuration is as specified on each component drawing/specification.**
 - **Workmanship standards have been met.**
 - **Test results are acceptable**



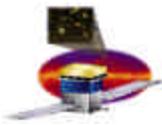
Material and Processes Program

- ❑ Calorimeter and its subcontractors will implement a materials and processes program as per SLAC LAT-SS-00107-1, LAT Mechanical Parts Plan, which includes maintaining an as-designed and as-built list for Inorganics and Metallics, Polymerics, Lubricants, and Processes.
- ❑ Each subcontractor/collaborator shall establish a Material Review Board (MRB) for materials usage and disposition of all nonconforming materials and processes.
- ❑ Conventional, heritage, and compliant material will be used to the maximum extent possible.
- ❑ Materials planned to be used will conform to 1.0% Total Mass Loss (TML) and 1.0% Vacuum Condensed Material (VCM) per NASA Specification.
- ❑ Vacuum Stability Characteristics of all non-compliant materials and parts used shall be determined either by test as per ASTM 595 or existing data.
- ❑ Thermal vacuum baking, curing at elevated temperatures and thermal bake-out will be used to accept otherwise non-compliant materials.



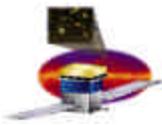
Contamination Control

- ❑ **Calorimeter contamination control program will be implemented as per LAT-MD-00228-D.**
- ❑ **Fabrication and integration of the Calorimeter Subsystem components will occur in a minimum of class 100,000 (per FED-STD-202).**
 - **Molecular witness plates shall be installed in the clean room at least two months before fabrication and assembly.**
 - **Particle witness plates (or equivalent automatic measurement system) shall also be implemented in the clean room.**
 - **Gowning protocol: hood, cleanroom gowns; boots; class 100,000 compatible gloves.**
 - **Assemblies containing crystals will be placed in nitrogen purge cabinets whenever stored for extended periods or there is a contamination threat in the local environment.**



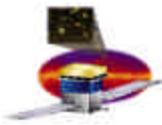
Contamination Control (2)

- ❑ Will document all cleaning processes and will not use solvents, materials or aids that would degrade a surface.
- ❑ Will review all manufacturing and integration processes for contamination hazards.
 - Will take protective measures (bagging, purging, pre-certification of facilities, etc.) necessary to prevent contamination especially during environmental testing.
 - Special emphasis on avoidance of contact transfer of molecular contaminant films (Fabrication Lubricants, Silicones, Human Oils).
- ❑ Surface cleanliness verification of flight hardware by optical witness samples, particle fallout plates, tape lifts, and/or NVR Rinses/Swabs.



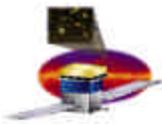
Contamination Control (3)

- On internal and external surfaces of Calorimeter, avoid the use of materials and processes that could generate particles, for example:
 - Paints (Overspray, Nodules), Fibrous Materials (Velcro lacing cord, metallic braid, unfinished composite edges, mesh), foams, vapor deposited thin films, dry lubricants, etc.
 - Drilling, soldering, abrading
 - Dissimilar metals, metallic surfaces without corrosion preventive finishes - especially aluminum.
 - Verify that polymers are thermally, UV and radiation stable.

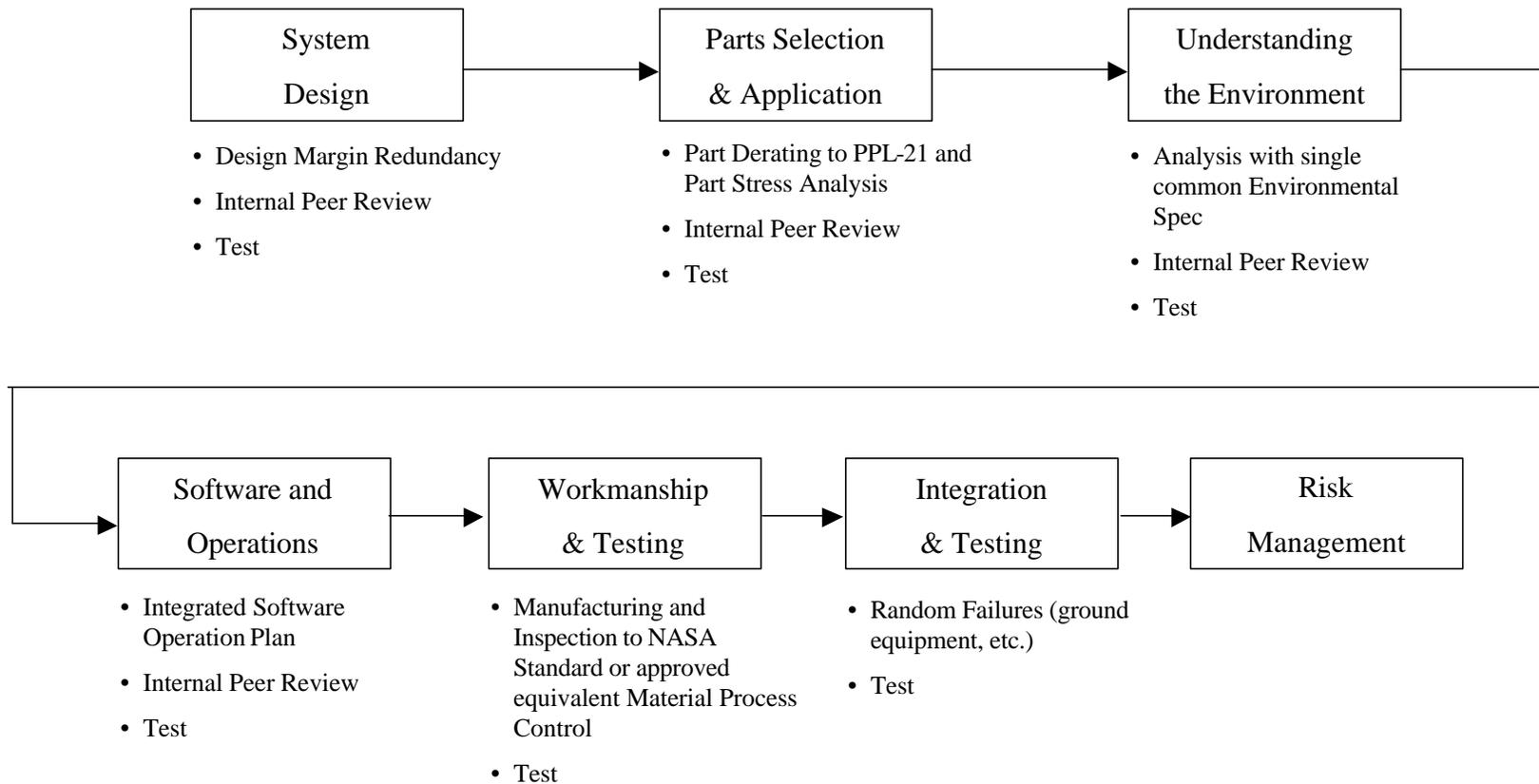


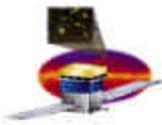
Reliability Program

- ❑ Calorimeter Subsystem has functional redundancy.
- ❑ Great Emphasis is placed on:
 - Robustness of DESIGN (class 2 level parts, derating, stress verification and risk analysis).
 - Applications where these parts are used are BENIGN.
 - MANUFACTURING Process Control and Workmanship inspection per NASA technical standards.
 - TESTING, Analysis and Simulations
 - Closed Loop Problem Anomaly Review, Continuous Risk Management and Disposition Process.
 - Everyone Including subcontractor must participate
 - Subsystems, Design, manufacturing, Test and Operations.



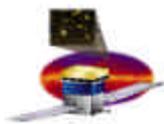
Reliability Program (2)



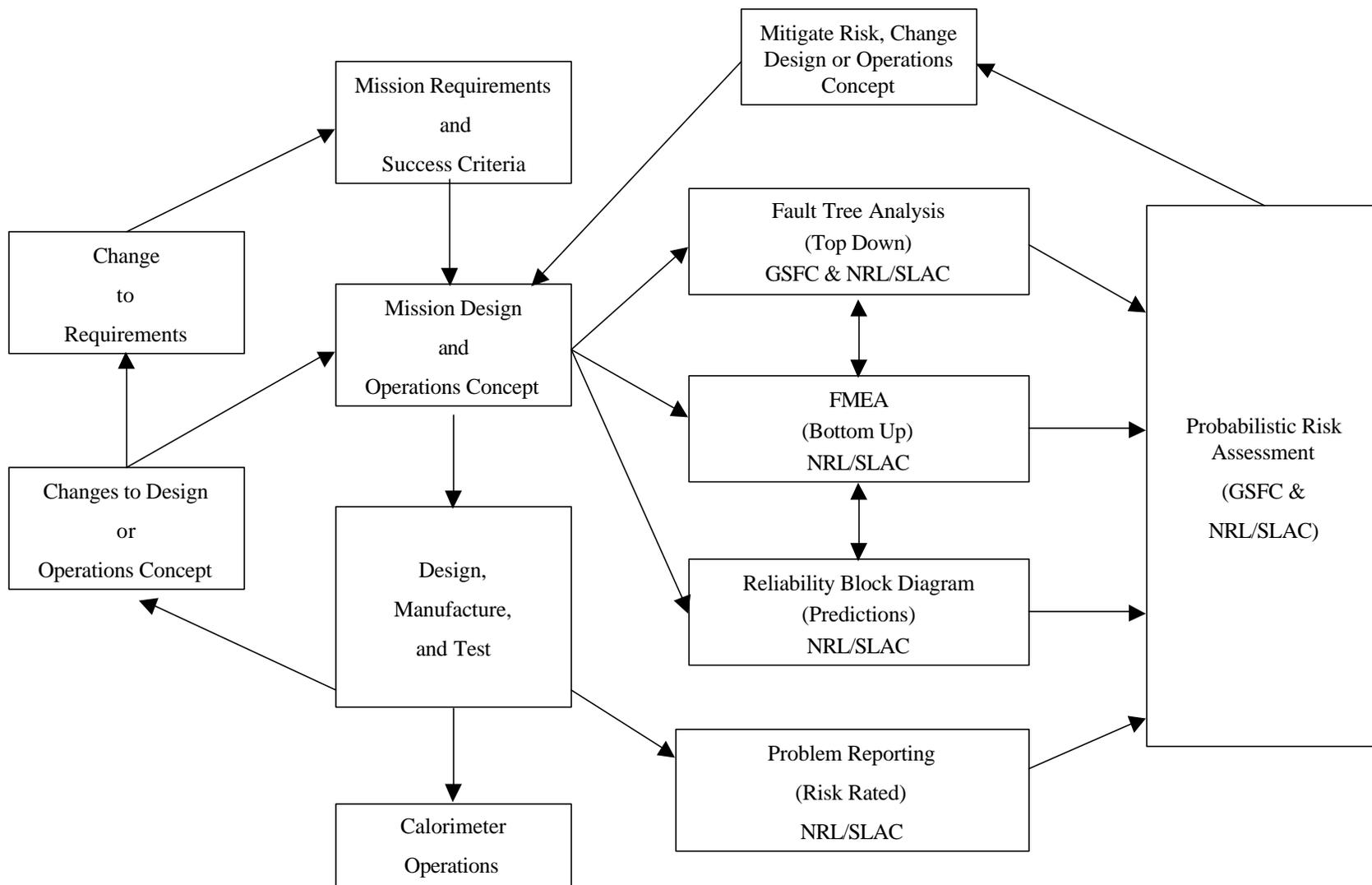


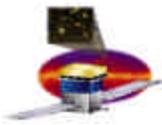
Reliability Program (3)

- ❑ **Single point failure scenarios and to take corrective action to mitigate the risk.**
- ❑ **Normal mode of operation will be considered.**
- ❑ **Loss of signal and presence of out-of-specification signal of each functional block will be addressed.**
- ❑ **Failure Modes and Effects Analysis, Fault Tree Analysis (LAT & GSFC), Reliability Predictions (LAT & GSFC), and Risk Assessment to identify mission ending failures, designs will be adjusted where possible to shift effect from “mission ending” to “degraded mission”.**
- ❑ **MIL-STD-1629 will be used as a guideline.**
- ❑ **Analysis on Calorimeter is being performed at the functional block level.**
- ❑ **Full theory of operation will be written for each functional block.**



Reliability Analysis Flow





Risk Management

- ❑ Continuous risk management will be performed as per LAT-MD-00236-D1, Calorimeter Risk Management Plan.
 - Flight and Ground element risks involve the end products performing their desired function in their operational environment.
 - FMEA, FTA, RBD and PRAs are good tools and will be used as required.
 - Project execution risk involves the ability to deliver the desired product meeting requirements, on time and within cost.
- ❑ To quantify risk, we will look at likelihood and consequence of an event
- ❑ Risk Management will include:
 - What can go wrong?
 - How will we know something has gone wrong?
 - When will we know that something has gone wrong?
 - What will we do about it?

**EXPECT THE UNEXPECTED SO THAT THE UNEXPECTED
BECOMES THE EXPECTED**

- ❑ These questions will be asked globally every day from design through manufacturing, test, and operations to assure mission success.



Failure Modes & Mitigations

Component	Possible cause or Failure type	Effect of failure	Criticality	Mitigation if failure occurs	Performance after mitigation	Allowable rate
CAL subsystem	Power; design flaw	No energy measurement. Loss of science.	2	None	No energy measurement. Loss of science.	None
CAL tower	TEM; power	>1/16 of data lost, CR rejection compromised	3	None. Modify E algorithms, bkg rejection algorithms.	>1/16 of data lost. CR rejection compromised. Energy measurement compromised.	None
CAL side	TEM i/f failure, cable failure; AFEE failure	~50% loss of measured energy in 48 logs (½ tower). Lose longitudinal position information in 48 logs. Lose redundancy in 48 logs. 25% loss of data volume from tower.	4	Modify E algorithm in ground s/w. Can be automated. Modify CAL-only direction measurements. Modify bkg rejection algorithms?	Resolution in 48 logs degraded to >5%. Lose longitudinal position information in 48 logs. Lose redundancy in 48 logs. 25% loss of data volume from tower.	One side
GCRC (Digital Controller)	Complete failure (power, chip)	~50% loss of measured energy in 12 logs. Lose longitudinal position information in 12 logs. Lose redundancy in 12 logs. 6% loss of data volume from tower.	4	Modify E algorithm in ground s/w. Can be automated.	Resolution in 12 logs degraded to >5%. Lose longitudinal position information in 12 logs. Lose redundancy. 6% loss of data volume from tower.	8 controllers, i.e. ~3% of CAL log ends.
GCFE chip	Component failure	~50% loss of measured energy in single log. Lose longitudinal position information in single log. Lose redundancy in single log. Negligible decrease in data volume (i.e. by 32 bits for only those events that should have involved the failed log).	4	Modify E algorithm in ground s/w. Can be automated.	Resolution in single log degraded to >5%. Lose longitudinal position information in single log. Lose redundancy in single log. Negligible decrease in data volume.	100 chips, i.e. 3% of CAL log ends.



Failure Modes & Mitigations (2)

Component	Possible cause or Failure type	Effect of failure	Criticality	Mitigation if failure occurs	Performance after mitigation	Allowable rate
CAL subsystem	Power; design flaw	No energy measurement. Loss of science.	2	None	No energy measurement. Loss of science.	None
GCFE chip	Failure of zero suppress	Increase data volume by one log (32 bits) for every event.	5	None?	Increase data volume by one log (32 bits) for every event.	300 chips (i.e. 10% increase in CAL data volume).
GCFE chip	Failure of autoranging	Miscalculated energy in single log?	4	None? Disable log face in flight?	Miscalculated energy in single log?	
GCFE energy range		~50% loss of measured energy over 1/4 of dynamic range in single log. Reduce redundancy in single log. Bias in auto-ranging in single log. Possible bias in longitudinal position information in single log.	4	Modify E algorithm in ground s/w. Can be automated.	Small increase in energy uncertainty in single log. Reduce redundancy in single log. Bias in auto-ranging in single log. Possible bias in longitudinal position information in single log.	100 ranges, i.e. ~3% of log ends.
ADC	Component failure	~50% loss of measured energy in single log. Lose longitudinal position information in single log. Lose redundancy in single log.	4	Modify E algorithm in ground s/w. Can be automated.	Resolution in single log degraded to >5%. Lose longitudinal position information in single log. Lose redundancy in single log.	100 chips, i.e. ~3% of log ends.
Dual PIN module	Open circuit, no signal	~50% loss of measured energy in single log. Lose longitudinal position information in single log. Lose redundancy in single log.	4	Modify E algorithm in ground s/w. Can be automated.	Resolution in single log degraded to >5%. Lose longitudinal position information in single log. Lose redundancy in single log.	100 dual PINs, i.e. ~3% of log ends.
Large PIN diode	Open circuit, no signal	~50% loss of measured energy <1.6 GeV in single log. Lose redundancy in single log.	4	Modify E algorithm in ground s/w. Can be automated.	Degrade longitudinal position information <1.6 GeV in single log.	100 PINs, i.e. ~3% of log ends.



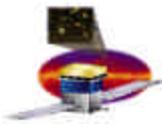
Failure Modes & Mitigations (3)

Component	Possible cause or Failure type	Effect of failure	Criticality	Mitigation if failure occurs	Performance after mitigation	Allowable rate
Small PIN diode	Open circuit, no signal	~50% loss of measured energy >1.6 GeV in single log. Lose redundancy >1.6 GeV in single log.	4	Modify E algorithm in ground s/w. Can be automated.	Resolution in single log degraded to >5% >1.6 GeV. Lose longitudinal position information >1.6 GeV in single log. Lose redundancy >1.6 GeV in single log.	100 PINs, i.e. ~3% of log ends.
Dual PIN module	Loss of bias	Increased noise, decreased resolution in single log.	5	Raise zero-suppress LLD	Decreased resolution in single log.	100 dual PINs, i.e. ~3% of log ends.
Large PIN diode	Loss of bias	Increased noise, decreased resolution in single log <1.6 GeV.	5	Raise zero-suppress LLD	Decreased resolution in single log <1.6 GeV.	100 PINs, i.e. ~3% of log ends.
Small PIN diode	Loss of bias	Increased noise, decreased resolution in single log >1.6 GeV.	5	None	Decreased resolution in single log >1.6 GeV.	100 PINs, i.e. ~3% of log ends.
Dual PIN module	Failed optical bond	~25% loss of measured energy in single log	5	Recalibrate with GCRs. Modify E algorithm in ground s/w.	Resolution in single log degraded to >TBD%.	100 dual PINs, i.e. ~3% of log ends.
Large PIN diode	Failed optical bond	~25% loss of measured energy <1.6 GeV in single log	5	Recalibrate with GCRs.	Resolution in single log degraded to >TBD%.	100 PINs, i.e. ~3% of log ends.
Small PIN diode	Failed optical bond	~25% loss of measured energy >1.6 GeV in single log.	5	Recalibrate with GCRs.	Resolution in single log degraded to >TBD%.	100 PINs, i.e. ~3% of log ends.



Failure Modes & Mitigations (4)

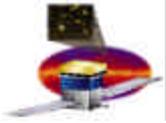
Component	Possible cause or Failure type	Effect of failure	Criticality	Mitigation if failure occurs	Performance after mitigation	Allowable rate
Calibration DAC	Component failure	Degraded E resolution in 1/2 of tower. Increased uncertainty at high end of HEX1 range.	5	None, but increased reliance on GCR calibration.	Degraded E resolution in 1/2 of tower. Increased uncertainty at high end of HEX1 range.	
CAL-LO Trigger, single tower		During I&T: Loss of ability to calibrate tower with muons. During flight: Loss of ability to use CAL-LO to throttle TKR trigger rate. Loss of ability to measure TKR trigger efficiency.	4	During I&T: Hardware replacement. During flight: None	Loss of ability to use CAL-LO to throttle TKR trigger rate. Loss of ability to measure TKR trigger efficiency.	16 towers? None?
CAL-HI Trigger, single tower		Reduced efficiency of CAL-only triggers. Reduced effective area at high energies.	4	None.	Reduced efficiency of CAL-only triggers. Reduced effective area at high energies.	
CAL-LO Trigger, single GCRC	Fail in asserted state	Rapid triggering, large data volume. Loss of CAL-LO trigger from several log faces.	4	Disable trigger from failed GCRC.	Loss of CAL-LO trigger from several log faces.	
CAL-HI Trigger, single GCRC	Fail in asserted state	Rapid triggering, large data volume. Loss of CAL-HI trigger from several log faces.	4	Disable trigger from failed GCRC.	Loss of CAL-HI trigger from several log faces.	



Performance Assurance

Major Areas of Performance Assurance

- ❑ Quality Program Management and Support Planning
- ❑ Design Reviews
- ❑ Procurement and Subcontractor Controls
- ❑ Quality Program Records
- ❑ Calibration Control System
- ❑ Manufacturing and Test Control
- ❑ In-process, inspection training and certification
- ❑ Non-Conformance material control
- ❑ Internal auditing
- ❑ Customer / Government Liaison



Manufacturing Quality Control

- ❑ Design Liaison
- ❑ Review of manufacturing processes.
- ❑ Review of assembly documentation.
- ❑ Review of manufacturing facilities personnel.
- ❑ Preparation of Work Order Authorization (WOA) and nonconformance Problem Record (PR) close loop system.



Work Order Authorization

Access Data Base Work Order Authorization Form

Microsoft Access
File Edit View Insert Format Records Tools Window Help

Work Order Authorization System

Page 1 of 1

WOA TITLE: _____ WOA NO.: _____

DATE OF REQUEST: _____ ORIGINATOR: _____ RESPONSIBLE PERSON: _____
 ORGANIZATION: _____ ORGANIZATION: _____
 EXPECTED END DATE: _____ PHONE NUMBER: _____ PHONE NUMBER: _____

SYSTEMS/SUBSYSTEM: _____ ITEM DESCRIPTION: _____

BRIEF DESCRIPTION OF WORK: _____

REQUIRED DOCUMENTS: _____ ACTIVITY LEVEL: NON-FLIGHT
 FLIGHT OTHER _____

HAZARDS/CONSTRAINTS: _____ PART NUMBERS: _____ SERIAL NUMBERS: _____

APPROVAL SIGNATURES:

SIGNATURE	APPVD	INITIALS	DATE
I&T MANAGER: _____	_____	_____	_____
MECHANICAL MANAGER: _____	_____	_____	_____
ELECTRICAL MANAGER: _____	_____	_____	_____
SYSTEMS MANAGER: _____	_____	_____	_____
QUALITY MANAGER: _____	_____	_____	_____
OTHER: _____	_____	_____	_____

REQUIRED SUPPORT:

QA WITNESS: YES NO
 QA FINAL INSPECTION: YES NO
 SAFETY: YES NO
 PHOTO: YES NO

CONFIGURATION MGMT STAMP & DATES:

PERFORMED BY	INSPECTION BY	PR ITEM #	CLOSE OUT BY
INITIALS	INITIALS		INITIALS
DATE	DATE		DATE
INITIALS	INITIALS		INITIALS

Submit Work Order for Approval

Record: 1 of 1

- Originator/Organization/Phone #
 - List of Names
- Responsible Person/Organization
 - List of Names
- System/Subsystem
 - List of Systems/Subsystems
- Description of Work
- Required Documents
- Activity Levels
 - Flight
 - Non-Flight
 - Other
- Part Numbers
- Serial Numbers
- Signature Column
 - List of Names
- Required Support



Work Order Authorization (2)

Access Data Base WOA Problem Record Form

Microsoft Access
File Edit View Insert Format Records Tools Window Help

Problem Record Form : Form

CHOOSE WOA: 1050
WOA NO: _____

WORK ORDER AUTHORIZATION PROBLEM RECORD

Open Work Order Info Open PR Assignment Rpt

SYSTEM/EXPERIMENT/INSTRUMENT		PROJECT / SYSTEM	TYPE OF HARDWARE		DRAWING / PART #	REV	SERIAL #	QTY
			<input type="checkbox"/> FLIGHT	<input type="checkbox"/> NON-FLIGHT				
			<input type="checkbox"/> OTHER _____					

NUMBER		PROBLEM DESCRIPTION	FOUND BY	DISPOSITION	DISPOSITION APPROVAL	Corrective Action Performed By	Quality Assurance
Event	PR #						
			INITIALS		QA <input type="checkbox"/>	INITIALS	INITIALS
			DATE		Eng <input type="checkbox"/>	DATE	DATE

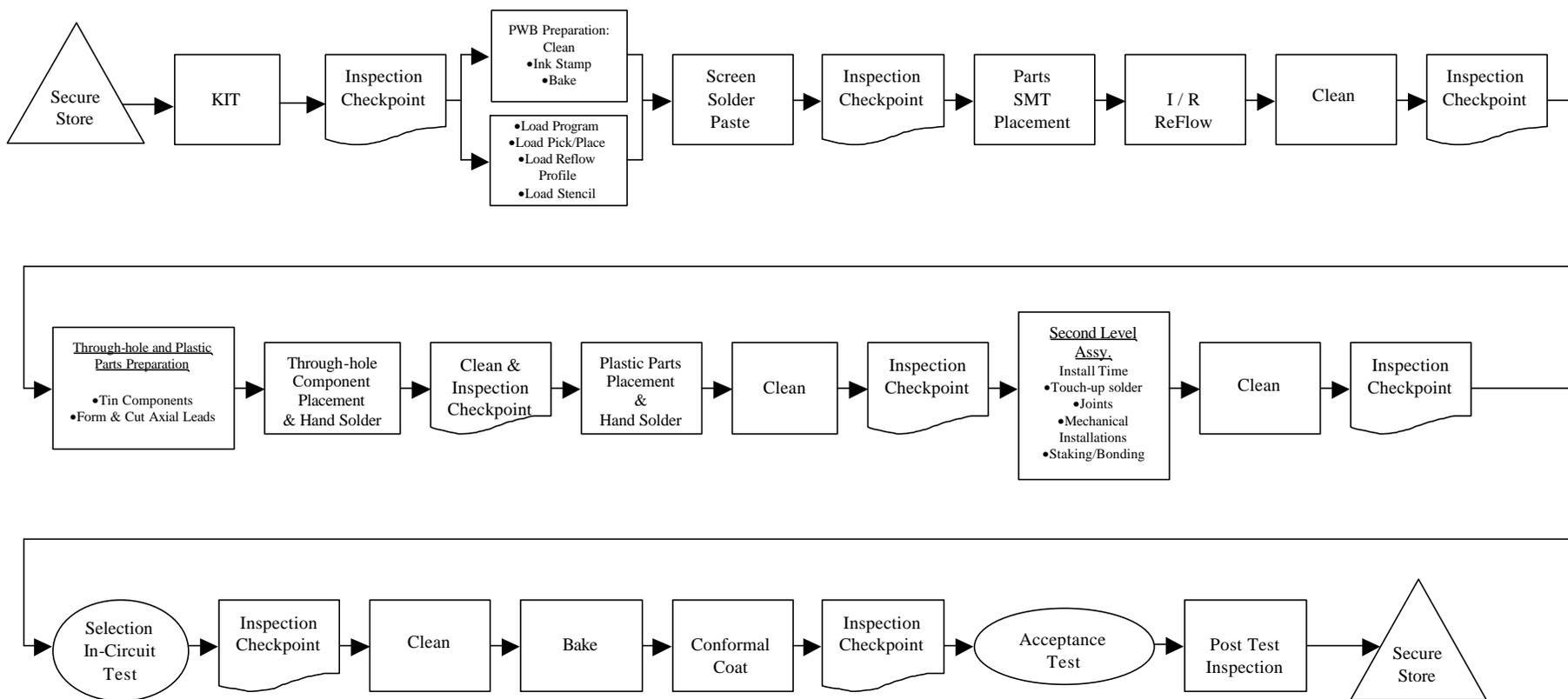
Form View FLTR

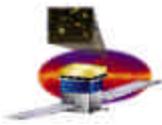
- Choose WOA
 - List of WOA Number
- Problem Record Status Code
 - Red - Critical Problem
 - Yellow - Urgent Problem
 - Green - Routine Problem
 - Risk Analysis & Categorization
- System/Subsystem
 - List of Systems/Subsystems
- Assigned To
 - List of Names
- Drawing Number
- Problem Disposition
- Corrective Action
- Type of Hardware
 - Flight
 - Non-Flight
 - Other
- Problem Description



PWB Manufacturing Flow

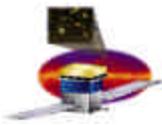
Typical manufacturing Flow Diagram of PWB Assembly





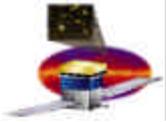
Software Quality Assurance

- ❑ Calorimeter subsystem program has the responsibility for ground software for testing of the subsystem.
- ❑ Software Assurance Program will be in accordance with LAT Flight Software Management Plan, SLAC LAT-MD-00104-1.
- ❑ CAL software engineers will work with LAT team during the design, development, and testing of flight software and will participate in software reviews.



Verification Requirements

- ❑ A verification program will be implemented to ensure that the Calorimeter instrument meets its requirements.
- ❑ Verification documentation will be reviewed which includes the following:
 - Verification matrix
 - Environmental Test matrix
 - Verification procedures
- ❑ Prepare a final Acceptance Data Package for Calorimeter.



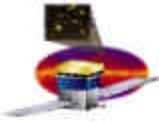
EM Development Schedule

W. Neil Johnson
Naval Research Laboratory



Development Program

- ❑ **PEM VM2 Prototype**
 - Mechanical Model w/ 12 CDE and 84 dummy crystals
 - CDE Performance testing before LAT PDR
 - Environmental testing completed by Dec '01
- ❑ **Front End Electronics**
 - GCFE Test Board – Radiation Testing - Nov '01
 - VM Board, GCFE + GCRC FPGA
 - Functional testing with CDE
 - Radiation testing – Jan '02
- ❑ **Engineering Model (EM)**
 - Form and function of flight units, commercial grade parts where required, fully populated PEM
 - Functional testing
 - Environmental testing
 - Beam tests
 - Delivered to SLAC for T&DF, software development



VM2 & EM Development

ID	Task Name	Duration	Start	Finish	2001												2002											
					J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	
4	VM Plan	41.8 wks	Thu 3/1/01	Tue 12/18/01	[Gantt bar from 3/1/01 to 12/18/01]																							
5	Xtal (15+1) delivery to F	0 days	Fri 6/29/01	Fri 6/29/01	[Task marker at 6/29]																							
6	Xtal metrology	5 days	Fri 6/29/01	Thu 7/5/01	[Task marker at 6/29]																							
7	Light yield test	10 days	Fri 7/6/01	Thu 7/19/01	[Task marker at 6/29]																							
8	NRL PIN delivery to F	0 days	Fri 8/24/01	Fri 8/24/01	[Task marker at 8/24]																							
9	PIN acceptance	2 days	Fri 8/24/01	Mon 8/27/01	[Task marker at 8/24]																							
10	French PINs delivery	0 days	Sun 9/2/01	Sun 9/2/01	[Task marker at 9/2]																							
11	F PIN acceptance	3 days	Mon 9/3/01	Wed 9/5/01	[Task marker at 9/2]																							
12	Preliminary Bonding Procedure available	0 days	Tue 8/14/01	Tue 8/14/01	[Task marker at 8/14]																							
13	CDE assembly	10 days	Thu 9/6/01	Wed 9/19/01	[Task marker at 8/14]																							
14	CDE Test	8 days	Thu 9/20/01	Mon 10/1/01	[Task marker at 8/14]																							
15	VM2 structure development	141 days	Thu 3/1/01	Thu 9/13/01	[Gantt bar from 3/1/01 to 9/13/01]																							
16	VM2 structure available	0 days	Fri 9/14/01	Fri 9/14/01	[Task marker at 9/14]																							
17	VM2 PEM Integration and Light Yield Test	6 days	Tue 10/2/01	Tue 10/9/01	[Task marker at 9/14]																							
18	VM AFEE	162 days	Thu 3/1/01	Fri 10/12/01	[Gantt bar from 3/1/01 to 10/12/01]																							
19	PDR prep / margin	14 days	Wed 10/10/01	Mon 10/29/01	[Task marker at 10/29]																							
20	LAT IPDR	0 days	Mon 10/29/01	Mon 10/29/01	[Task marker at 10/29]																							
21	VM2 PEM Env Test - ISSUE	50 days	Wed 10/10/01	Tue 12/18/01	[Gantt bar from 10/10/01 to 12/18/01]																							
22	EM plan	52.4 wks	Tue 8/14/01	Wed 8/14/02	[Gantt bar from 8/14/01 to 8/14/02]																							
23	EM PEM	29.4 wks	Tue 8/14/01	Wed 3/6/02	[Gantt bar from 8/14/01 to 3/6/02]																							
24	EM Structure available	0 days	Fri 12/21/01	Fri 12/21/01	[Task marker at 12/21]																							
25	PINs diodes available	0 days	Tue 10/9/01	Tue 10/9/01	[Task marker at 10/9]																							
26	Bonding Procedure finalized ?? San	0 days	Tue 8/14/01	Tue 8/14/01	[Task marker at 8/14]																							
27	Xtal delivery to F (>96 logs) date?	5 wks	Mon 9/17/01	Fri 10/19/01	[Task marker at 8/14]																							
28	CDE assembly & test	54 days	Mon 10/22/01	Thu 1/3/02	[Task marker at 8/14]																							
29	Clean room ready	1 day	Mon 12/31/01	Mon 12/31/01	[Task marker at 8/14]																							
30	EM PEM assembly (logs insert)	16 days	Fri 1/4/02	Fri 1/25/02	[Task marker at 8/14]																							
31	EM PEM assembly (closeouts)	1 day	Mon 1/28/02	Mon 1/28/02	[Task marker at 8/14]																							
32	EM PEM test (muon, light yield (Poly	22 days	Tue 1/29/02	Wed 2/27/02	[Task marker at 8/14]																							
33	Transportation F-NRL	5 days	Thu 2/28/02	Wed 3/6/02	[Task marker at 8/14]																							
34	EM A&T	43.6 wks	Mon 10/15/01	Wed 8/14/02	[Gantt bar from 10/15/01 to 8/14/02]																							
35	EM AFEE development	100 days	Mon 10/15/01	Fri 3/1/02	[Gantt bar from 10/15/01 to 3/1/02]																							
36	EM AFEE available (-digital ASIC?)	0 days	Mon 3/4/02	Mon 3/4/02	[Task marker at 3/4]																							
37	EM PEM available @ NRL	0 days	Fri 3/15/02	Fri 3/15/02	[Task marker at 3/15]																							
38	PEM acceptance	10 days	Mon 3/18/02	Fri 3/29/02	[Task marker at 3/15]																							
39	EM assembly	30 days	Mon 4/1/02	Fri 5/10/02	[Task marker at 3/15]																							
40	EM test	10 days	Mon 5/13/02	Fri 5/24/02	[Task marker at 3/15]																							
41	EM Env Test	28 days	Mon 5/27/02	Wed 7/3/02	[Task marker at 3/15]																							
42	Beam Test (hadrons)	30 days	Thu 7/4/02	Wed 8/14/02	[Task marker at 3/15]																							
43	CAL CDR	0 days	Wed 6/5/02	Wed 6/5/02	[Task marker at 6/5]																							
44	I-CDR	0 wks	Mon 8/5/02	Mon 8/5/02	[Task marker at 8/5]																							